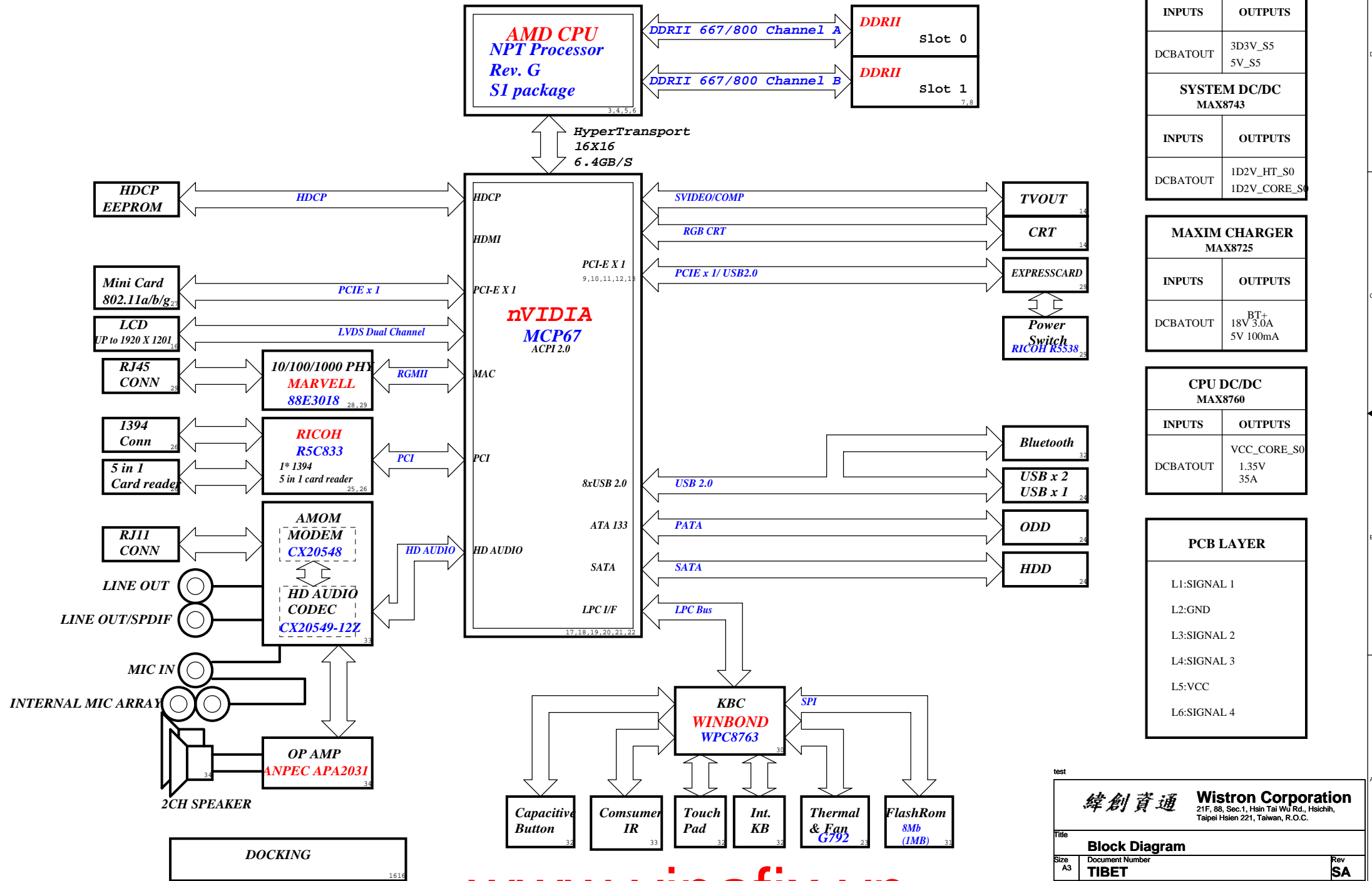
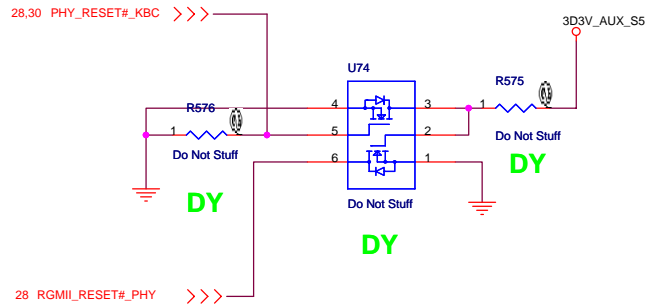
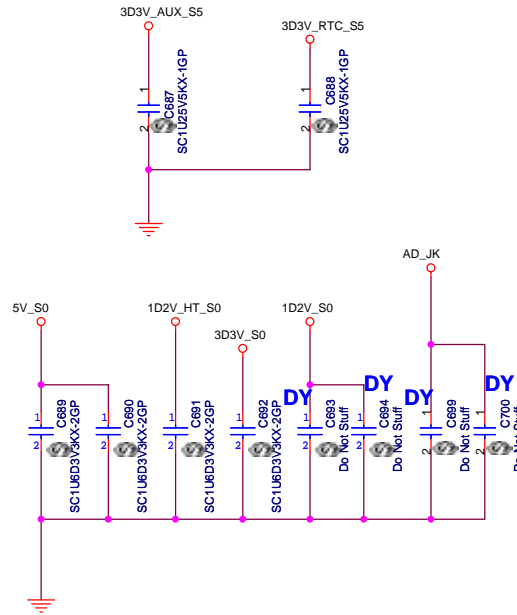
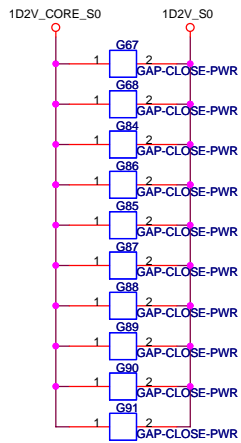


# Tibet Block Diagram





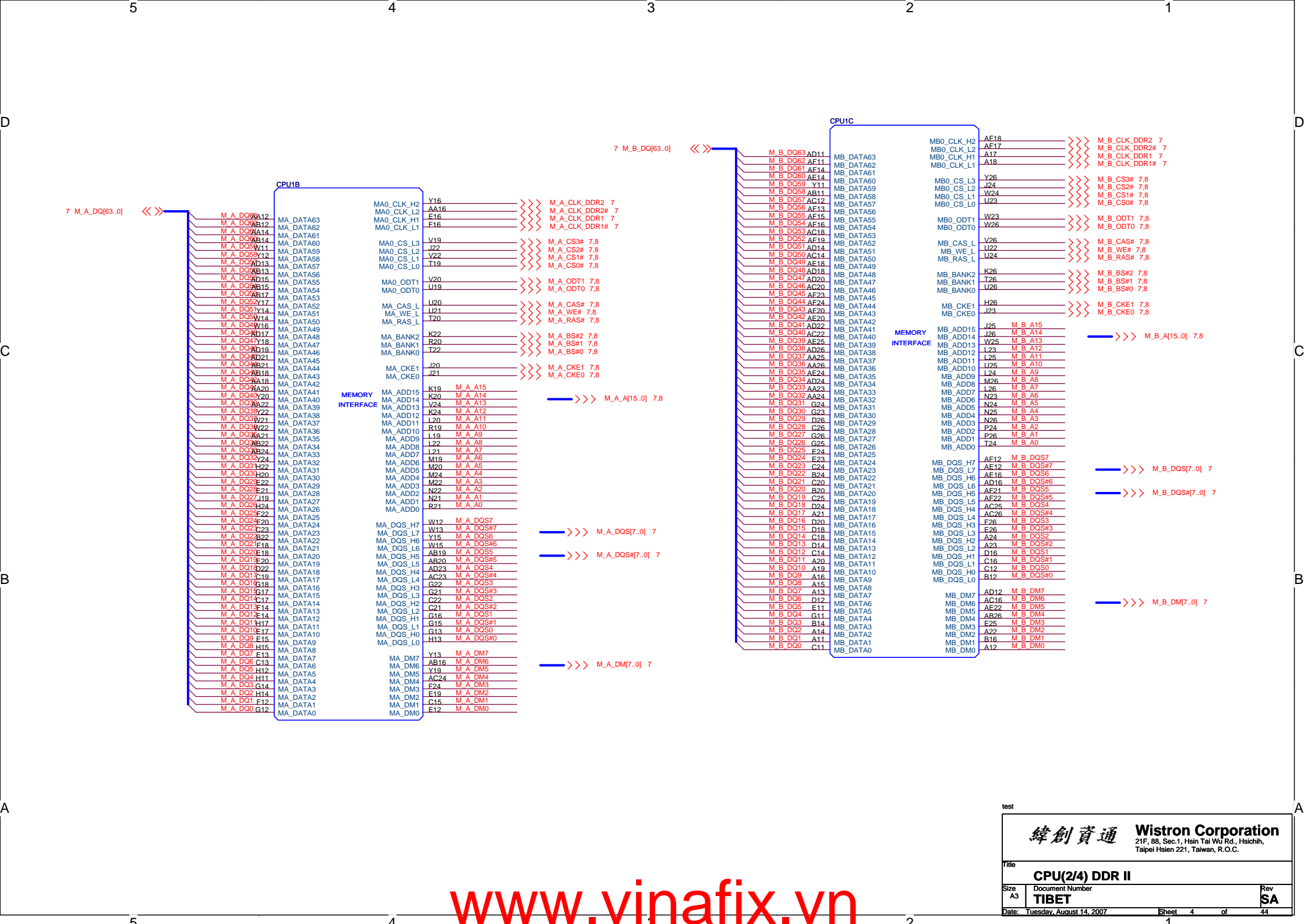
test

<b>緯創資通</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Size A3	Document Number <b>TIBET</b>	Rev <b>SA</b>
Date: Tuesday, August 14, 2007		
Sheet 2 of 44		

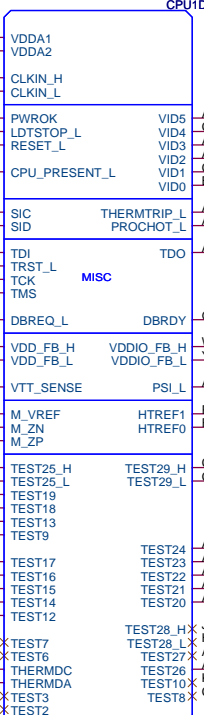
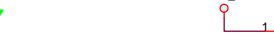


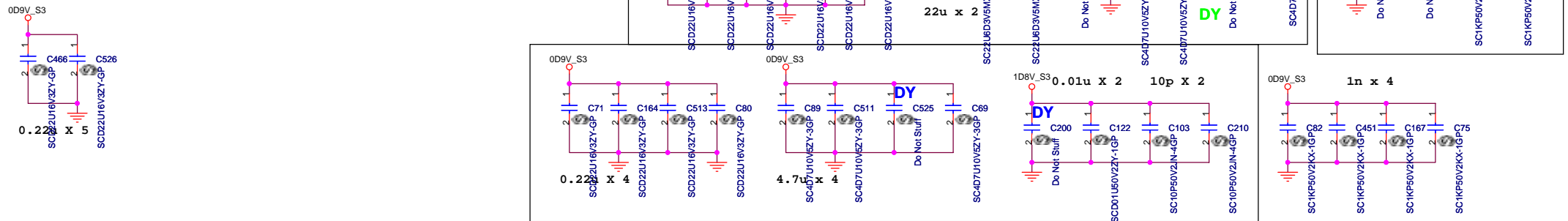
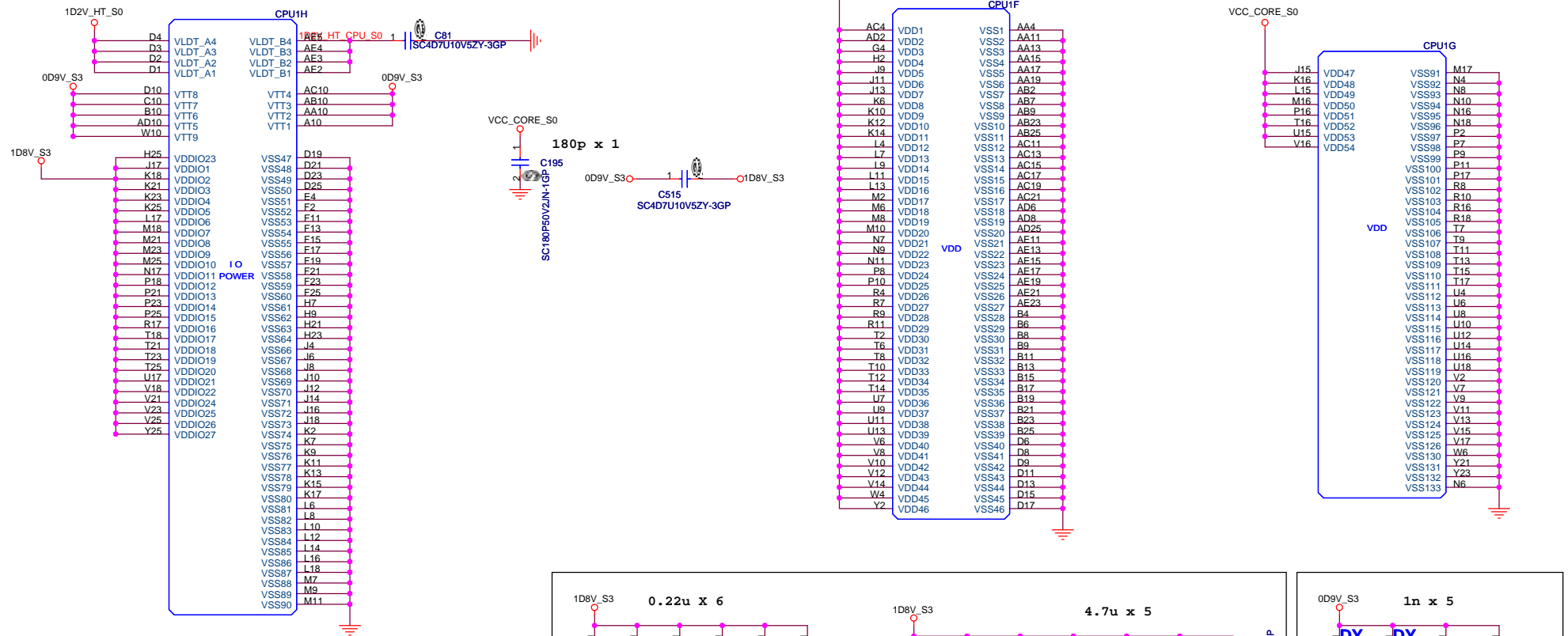
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<b>緯創資通</b> <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b> <b>CPU(1/4) HT</b>	
<b>Size</b> A3	<b>Document Number</b> <b>TIBET</b>
<b>Date:</b> Tuesday, August 14, 2007	<b>Rev</b> <b>SA</b>
<b>Sheet</b> 3	<b>of</b> 44

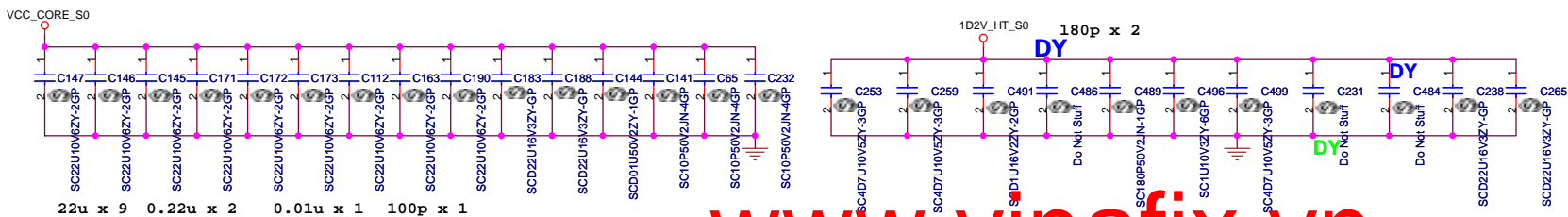


test





**LAYOUT:** Place on backside of processor.

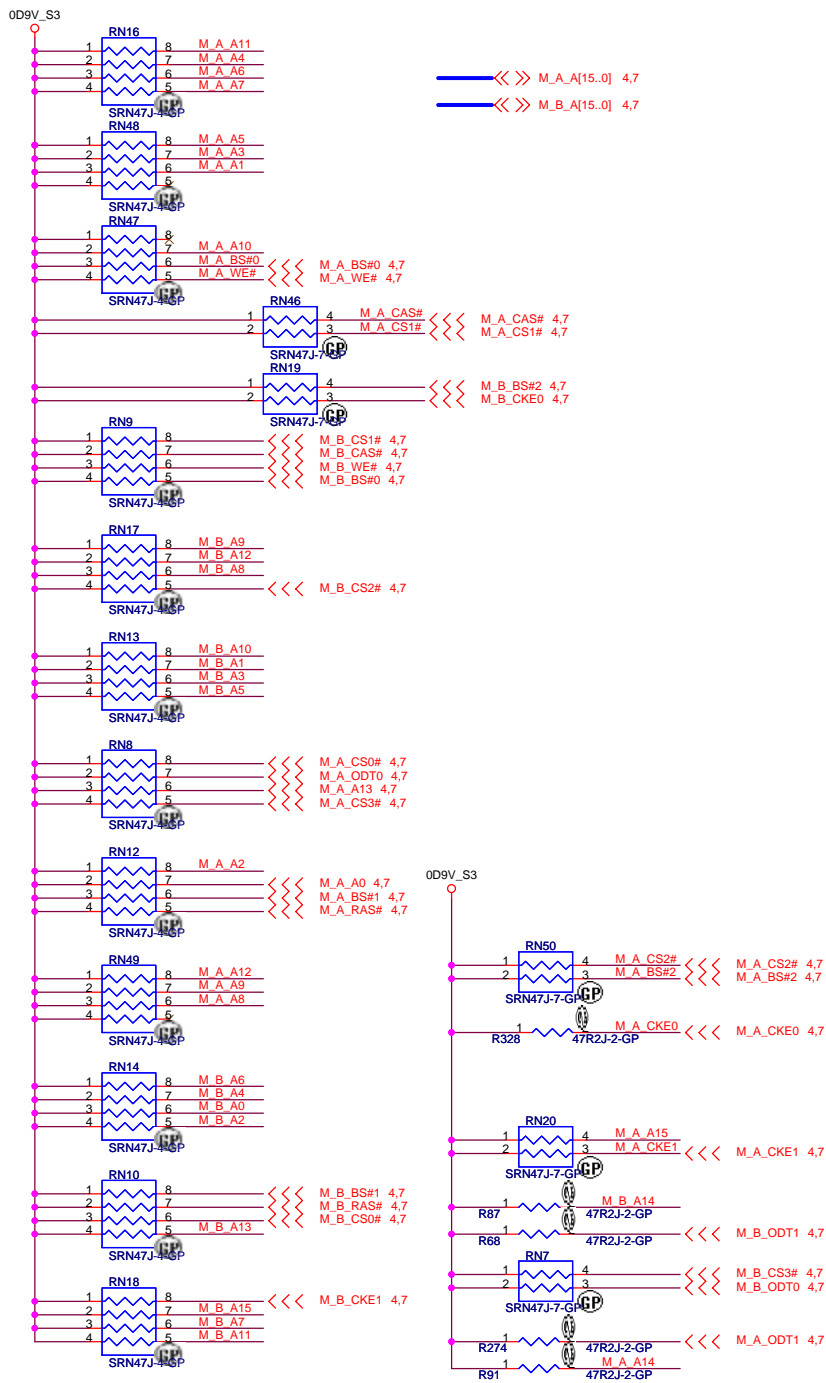






## PARALLEL TERMINATION

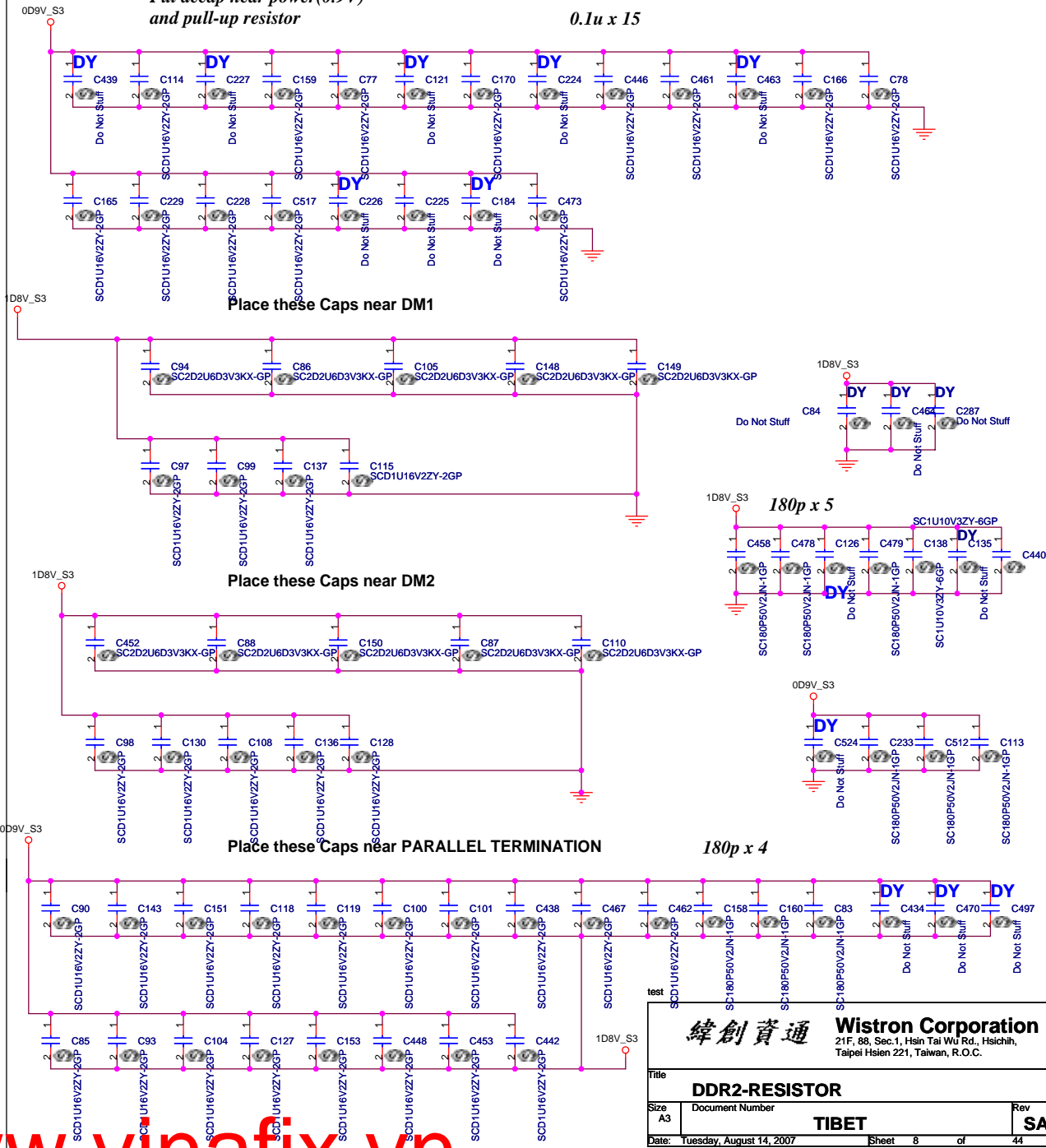
*Put decap near power(0.9V) and pull-up resistor*



## Decoupling Capacitor

*Put decap near power(0.9V)  
and pull-up resistor*

*0.1u x 15*



緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			
DDR2-RESISTOR			
Size A3	Document Number		Rev
	TIBET		SA
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CPUCADOUT[15..0] 3  
CPUCADOUTJ[15..0] 3

NB0CADOUT[15..0] 3  
NB0CADOUTJ[15..0] 3

U55A 1 OF 8

HT

CPUCADOUT0 AF16  
CPUCADOUTJ0 AG16  
CPUCADOUT1 AH16  
CPUCADOUTJ1 AJ16  
CPUCADOUT2 AJ15  
CPUCADOUTJ2 AK15  
CPUCADOUT3 AK16  
CPUCADOUTJ3 AL16  
CPUCADOUT4 AG17  
CPUCADOUTJ4 AF17  
CPUCADOUT5 AL17  
CPUCADOUTJ5 AK17  
CPUCADOUT6 AL18  
CPUCADOUTJ6 AK18  
CPUCADOUT7 AJ19  
CPUCADOUTJ7 AK19  
CPUCADOUT8 AD14  
CPUCADOUTJ8 AE14  
CPUCADOUT9 AF14  
CPUCADOUTJ9 AG14  
CPUCADOUT10 AH14  
CPUCADOUTJ10 AJ14  
CPUCADOUT11 AL13  
CPUCADOUTJ11 AK13  
CPUCADOUT12 AD15  
CPUCADOUTJ12 AE15  
CPUCADOUT13 AD16  
CPUCADOUTJ13 AE16  
CPUCADOUT14 AE17  
CPUCADOUTJ14 AD17  
CPUCADOUT15 AB17  
CPUCADOUTJ15 AC17

HT\_MCP\_RXD0\_P AK27  
HT\_MCP\_RXD0\_N AJ27  
HT\_MCP\_RXD1\_P AK26  
HT\_MCP\_RXD1\_N AL26  
HT\_MCP\_RXD2\_P AK25  
HT\_MCP\_RXD2\_N AL25  
HT\_MCP\_RXD3\_P AK24  
HT\_MCP\_RXD3\_N AL24  
HT\_MCP\_RXD4\_P AK22  
HT\_MCP\_RXD4\_N AL22  
HT\_MCP\_RXD5\_P AK21  
HT\_MCP\_RXD5\_N AL21  
HT\_MCP\_RXD6\_P AH21  
HT\_MCP\_RXD6\_N AJ21  
HT\_MCP\_RXD7\_P AL20  
HT\_MCP\_RXD7\_N AM20  
HT\_MCP\_RXD8\_P AG27  
HT\_MCP\_RXD8\_N AH27  
HT\_MCP\_RXD9\_P AE25  
HT\_MCP\_RXD9\_N AG25  
HT\_MCP\_RXD10\_P AH25  
HT\_MCP\_RXD10\_N AJ25  
HT\_MCP\_RXD11\_P AE23  
HT\_MCP\_RXD11\_N AD23  
HT\_MCP\_RXD12\_P AD21  
HT\_MCP\_RXD12\_N AE21  
HT\_MCP\_RXD13\_P AE21  
HT\_MCP\_RXD13\_N AG21  
HT\_MCP\_RXD14\_P AC20  
HT\_MCP\_RXD14\_N AD20  
HT\_MCP\_RXD15\_P AE19  
HT\_MCP\_RXD15\_N AE19

NB0CADOUT0 AK27  
NB0CADOUTJ0 AJ27  
NB0CADOUT1 AK26  
NB0CADOUTJ1 AL26  
NB0CADOUT2 AK25  
NB0CADOUTJ2 AL25  
NB0CADOUT3 AK24  
NB0CADOUTJ3 AL24  
NB0CADOUT4 AK22  
NB0CADOUTJ4 AL22  
NB0CADOUT5 AK21  
NB0CADOUTJ5 AL21  
NB0CADOUT6 AH21  
NB0CADOUTJ6 AJ21  
NB0CADOUT7 AL20  
NB0CADOUTJ7 AM20  
NB0CADOUT8 AG27  
NB0CADOUTJ8 AH27  
NB0CADOUT9 AE25  
NB0CADOUTJ9 AG25  
NB0CADOUT10 AH25  
NB0CADOUTJ10 AJ25  
NB0CADOUT11 AE23  
NB0CADOUTJ11 AD23  
NB0CADOUT12 AD21  
NB0CADOUTJ12 AE21  
NB0CADOUT13 AE21  
NB0CADOUTJ13 AG21  
NB0CADOUT14 AC20  
NB0CADOUTJ14 AD20  
NB0CADOUT15 AE19  
NB0CADOUTJ15 AE19

3 CPUHTTCLKOUT0 CPUHTTCLKOUT0 AJ17  
3 CPUHTTCLKOUTJ0 CPUHTTCLKOUTJ0 AH17  
3 CPUHTTCLKOUT1 CPUHTTCLKOUT1 AL14  
3 CPUHTTCLKOUTJ1 CPUHTTCLKOUTJ1 AK14

HT\_MCP\_RX\_CLK0\_P AK23  
HT\_MCP\_RX\_CLK0\_N AJ23  
HT\_MCP\_RX\_CLK1\_P AG23  
HT\_MCP\_RX\_CLK1\_N AH23

NB0HTTCLKOUT0 3  
NB0HTTCLKOUTJ0 3  
NB0HTTCLKOUT1 3  
NB0HTTCLKOUTJ1 3

3 CPUHTTCTLOUT0 CPUHTTCTLOUT0 AH19  
3 CPUHTTCTLOUTJ0 CPUHTTCTLOUTJ0 AG19  
RESERVED#AC18  
RESERVED#AD18

HT\_MCP\_TXCTL0\_P AK20  
HT\_MCP\_TXCTL0\_N AJ20  
RESERVED#AD19  
RESERVED#AC19

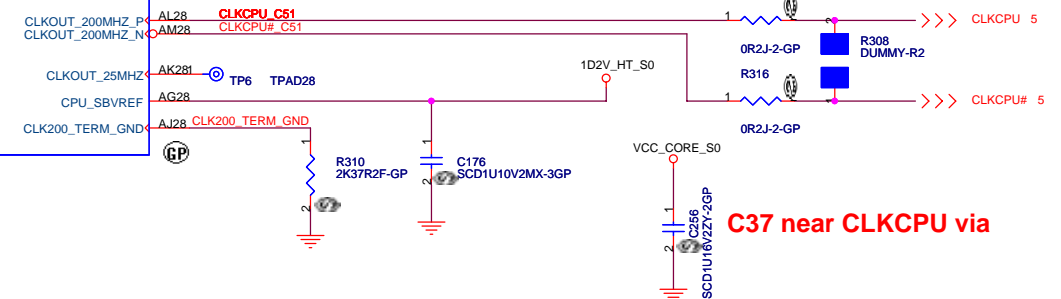
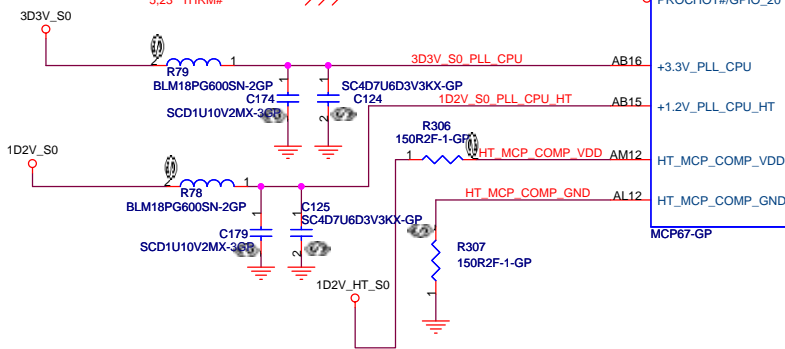
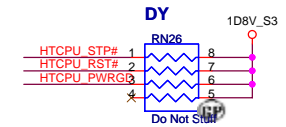
NB0HTTCTLOUT 3  
NB0HTTCTLOUTJ 3

5 CPU\_THERMTRIP# 5.23 THRM#

THERMTRIP#/GPIO\_58  
PROCOT#/GPIO\_20

HT\_MCP\_REQ# AD23  
HT\_MCP\_STOP# AB20  
HT\_MCP\_RST# AC21  
HT\_MCP\_PWRGD AD22

HT\_CPU\_REQ# 1  
HT\_CPU\_STOP# 5  
HT\_CPU\_RST# 5  
HT\_CPU\_PWRGD 5



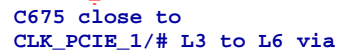
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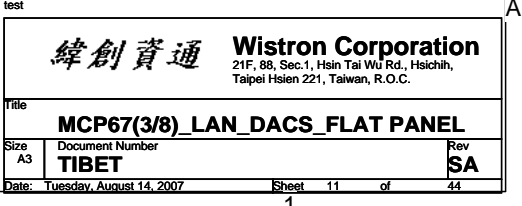
緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

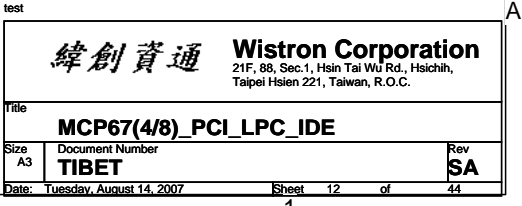
Title MCP67(1/8) HT CPU

Size A3 Document Number TIBET Rev SA

Date: Tuesday, August 14, 2007 Sheet 9 of 44



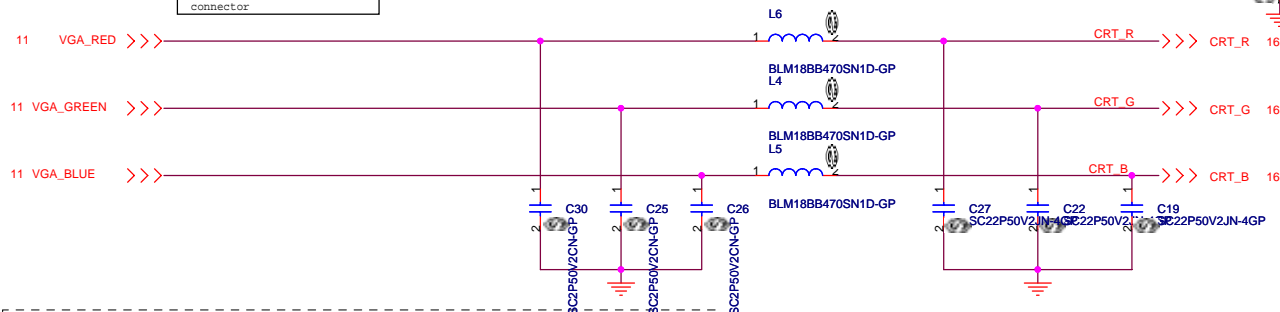






# CRT I/F & CONNECTOR

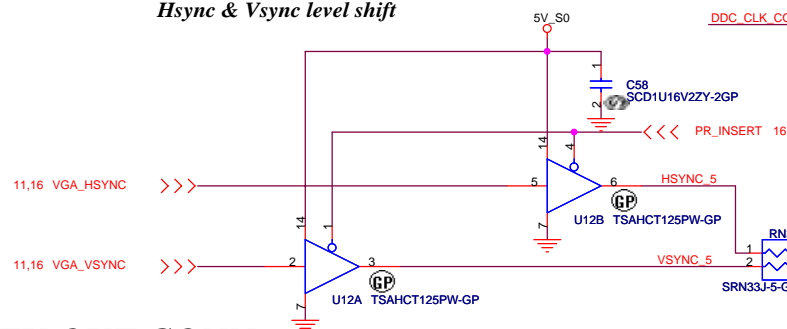
Layout Note:  
Place these resistors  
close to the CRT-out  
connector



## Layout Note:

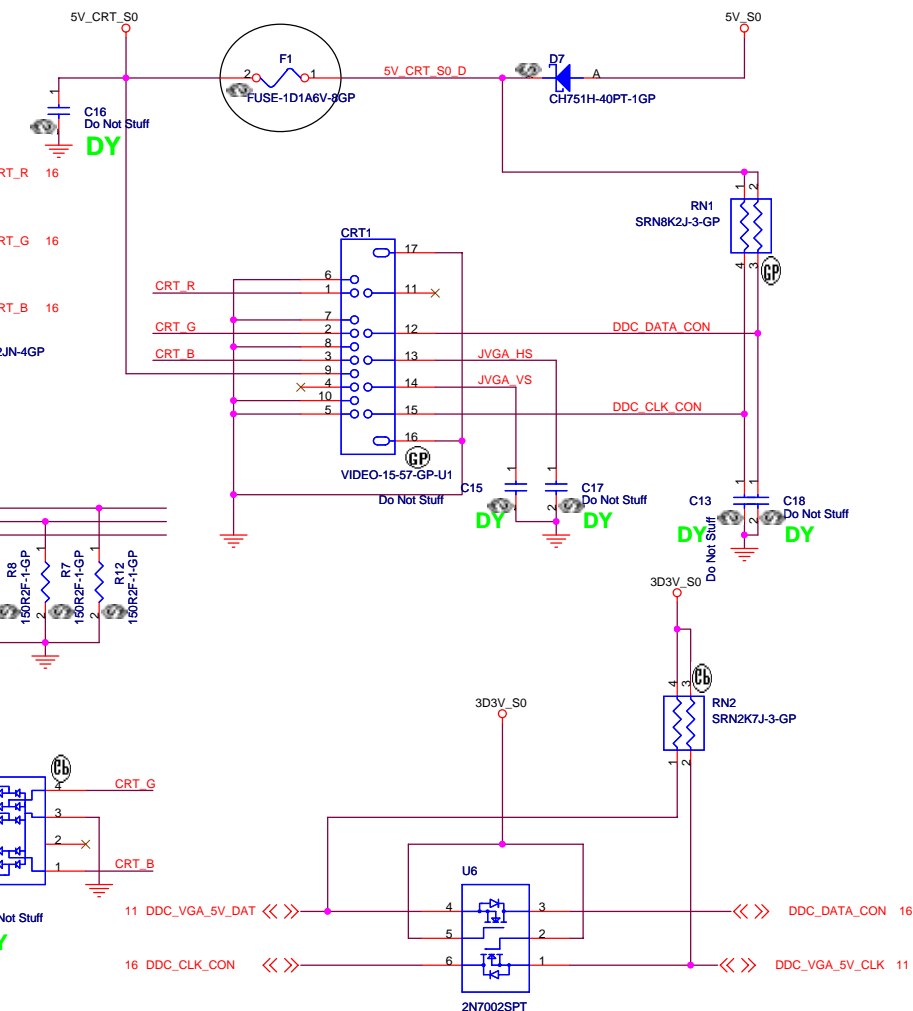
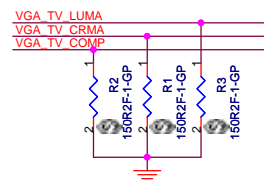
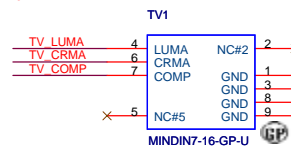
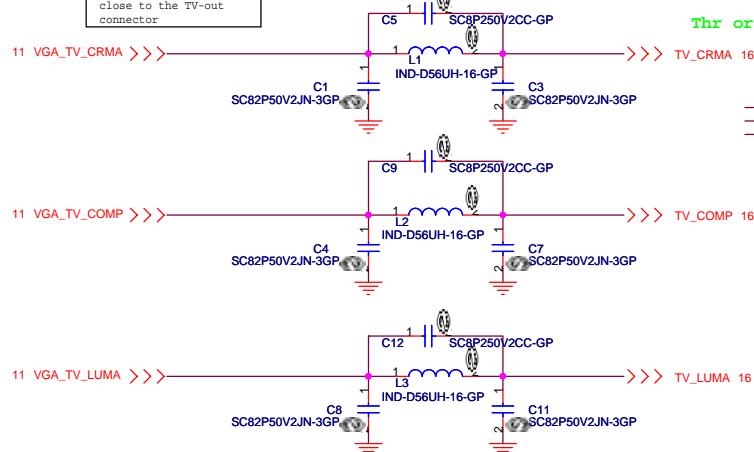
\* Must be a ground return path between this ground and the ground on the VGA connector.  
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

## Hsync & Vsync level shift



## TV OUT CONN

Layout Note:  
Place this 2 resistors  
close to the TV-out  
connector



5V @ ext. CRT side

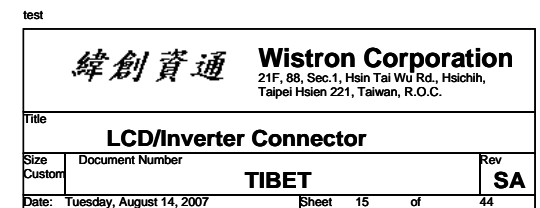
test

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Taipei Hsien 221, Taiwan, R.O.C.

CRT/TV CONNECTOR		
Size A3	Document Number	Rev SA
Date: Tuesday, August 14, 2007	Sheet 14 of 44	



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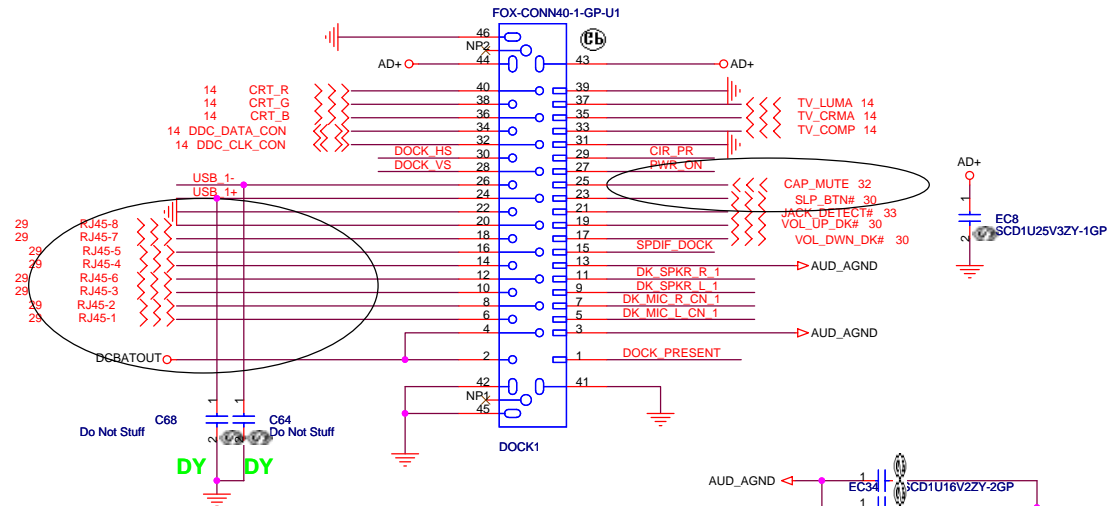
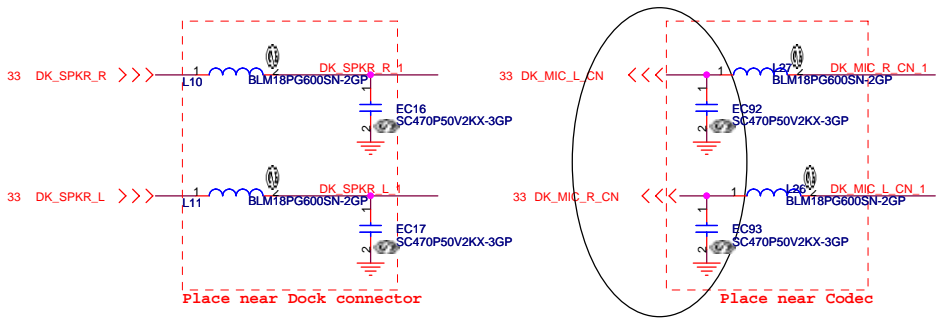
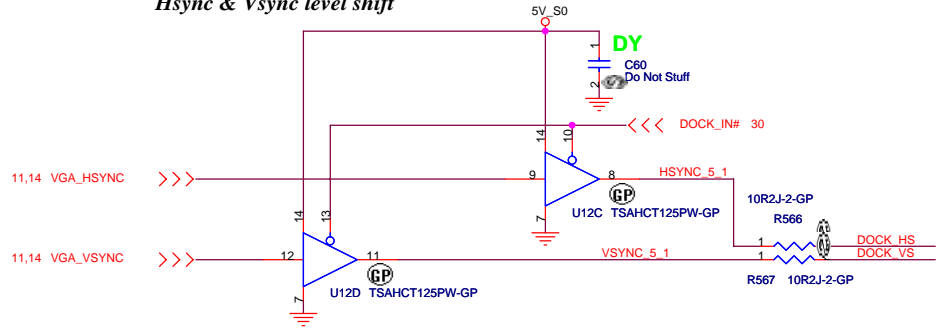




# Docking Connector

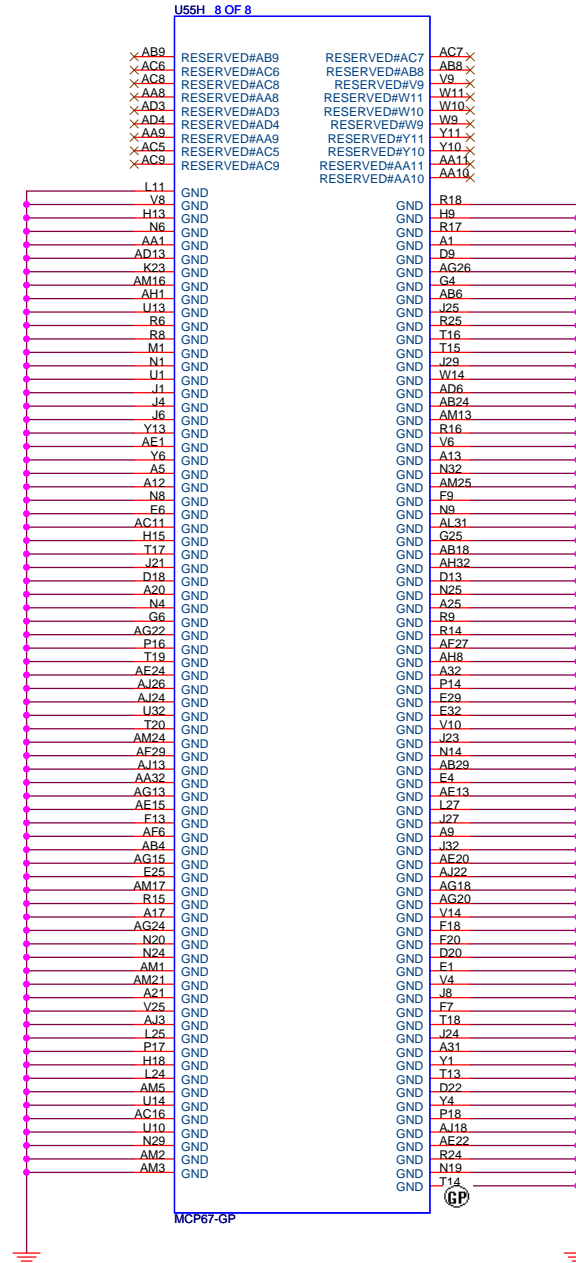


## Hsync & Vsync level shift



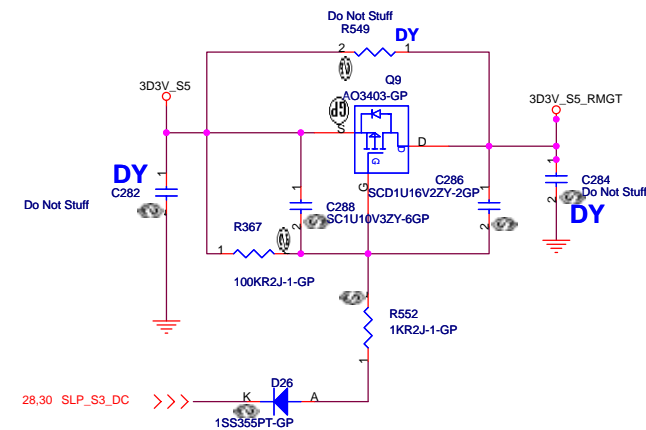
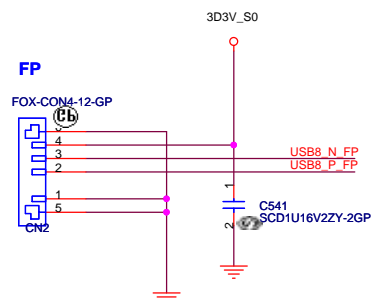
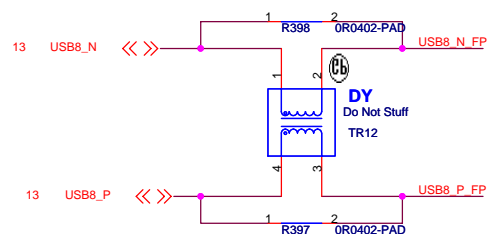
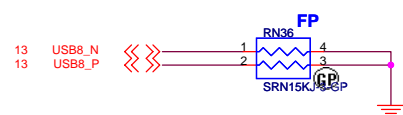
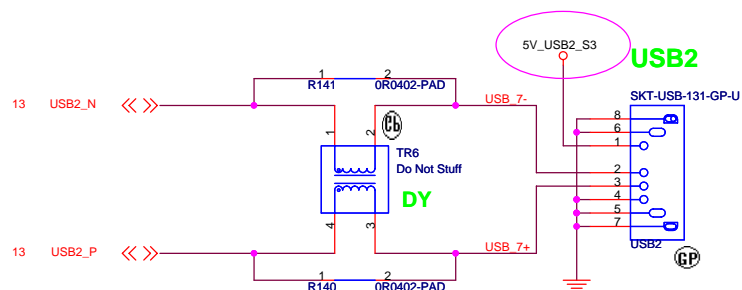
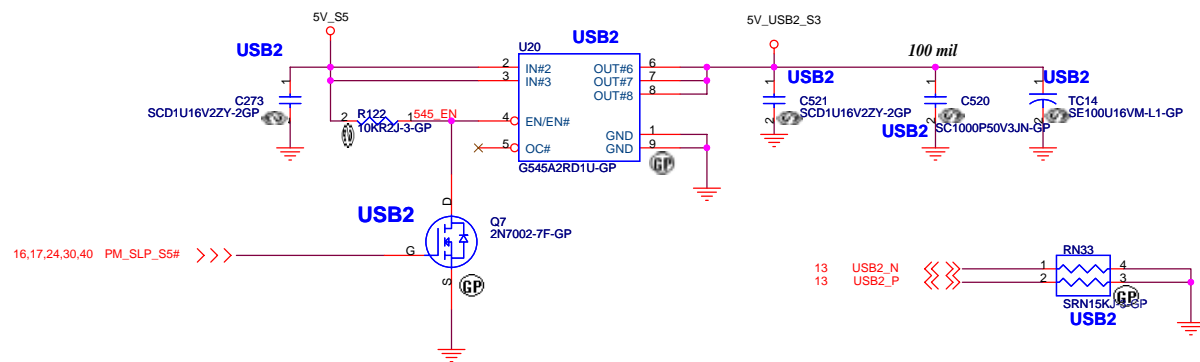




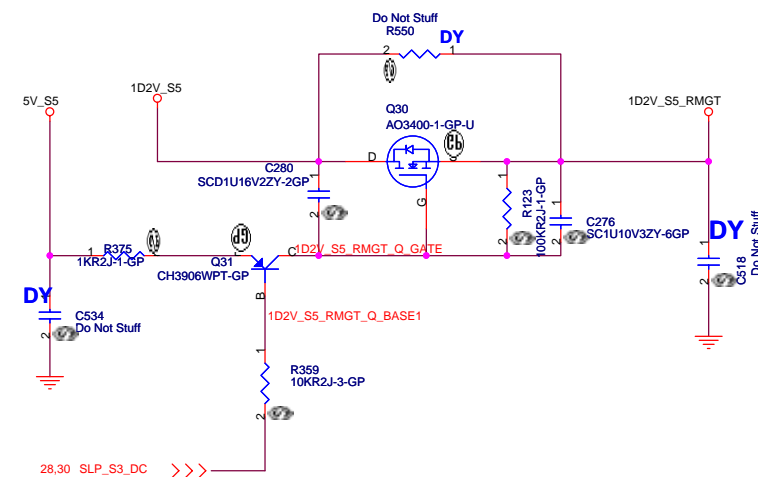


test

<b>緯創資通</b> <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>MCP67(8/8)_GND</b>	
Size A3	Document Number <b>TIBET</b>
Date: Tuesday, August 14, 2007	Rev <b>SA</b>
Sheet 19 of 44	



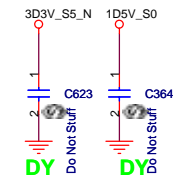
### ??? Current Rating



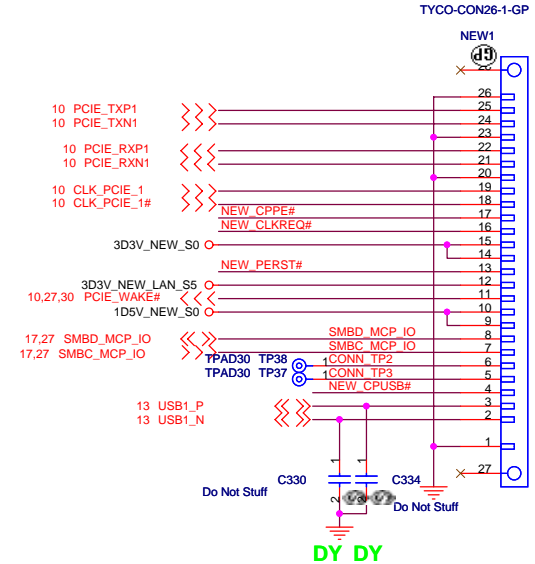
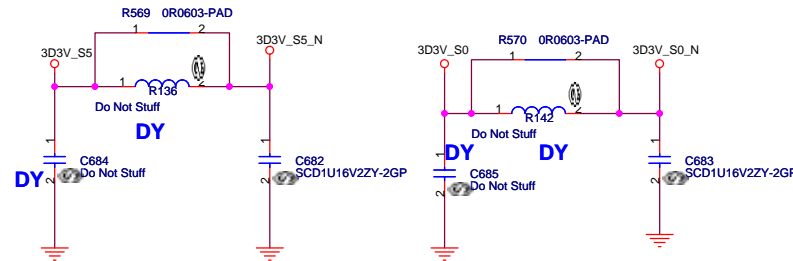
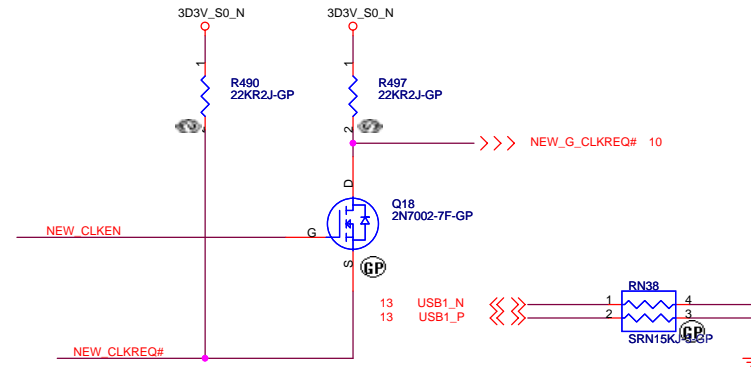
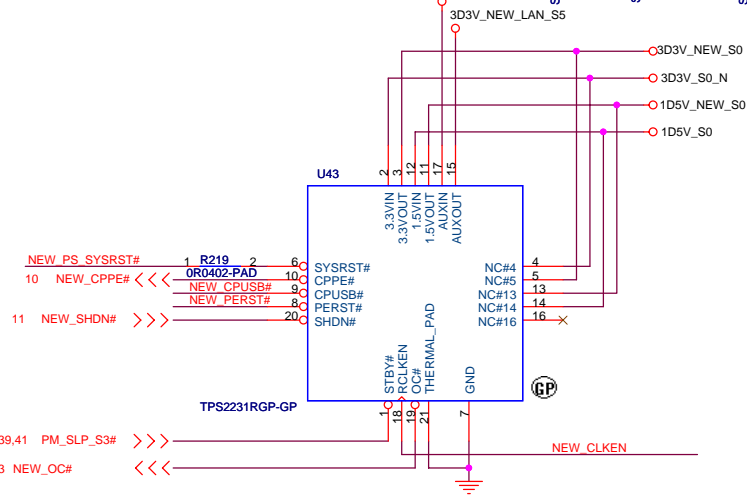
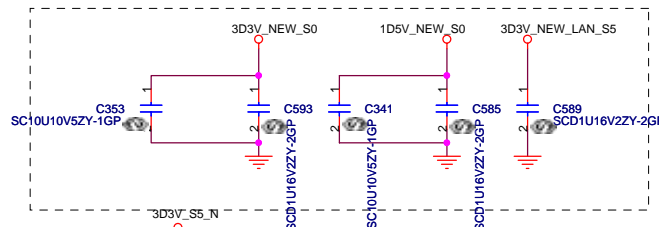


# NEWCARD Connector

Place them Near to Chip



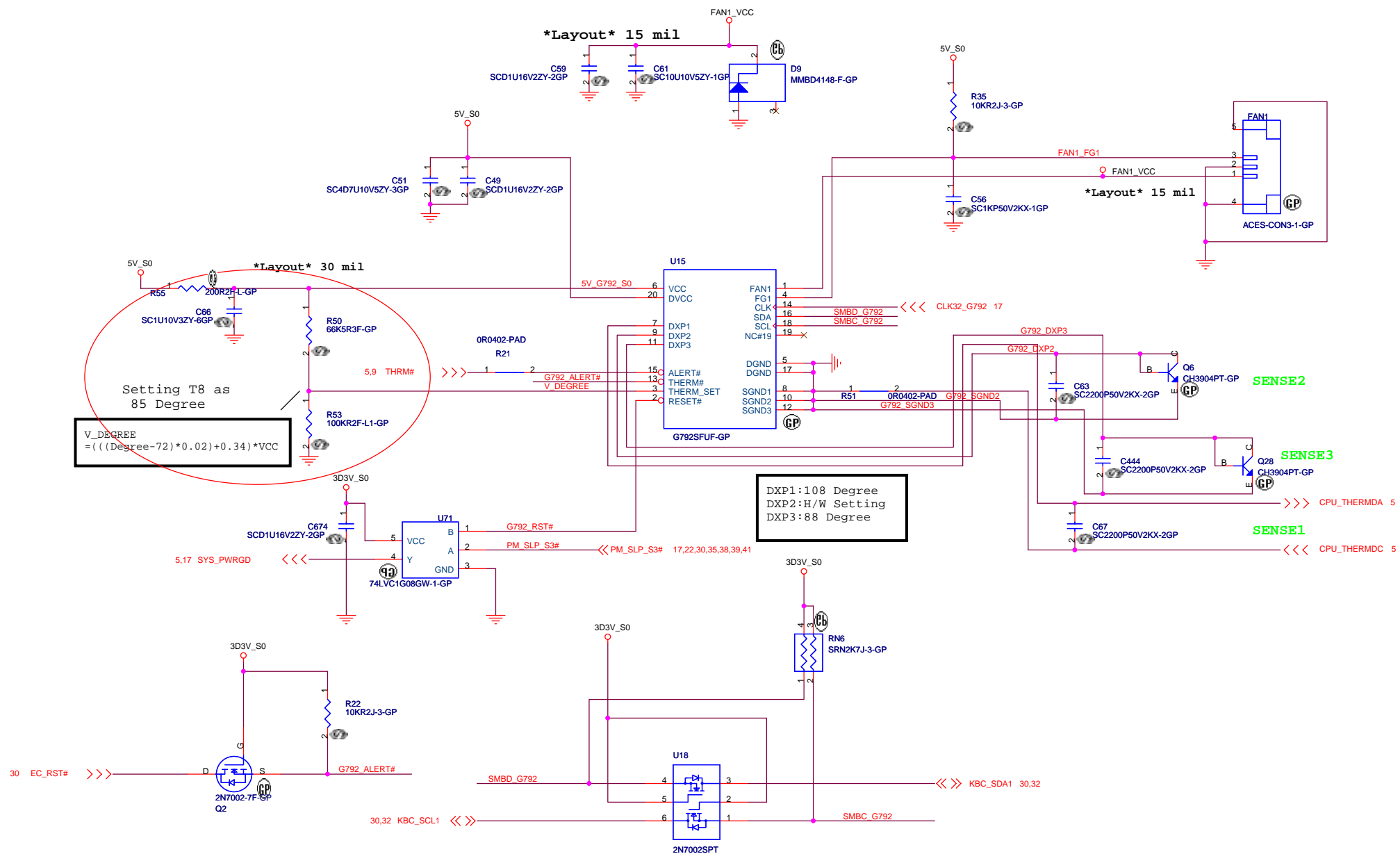
Place them Near to Connector



test

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Title			
NEW CARD			
Size	Document Number	Rev	
A3	TIBET	SA	
Date:	Tuesday, August 14, 2007	Sheet	22 of 44

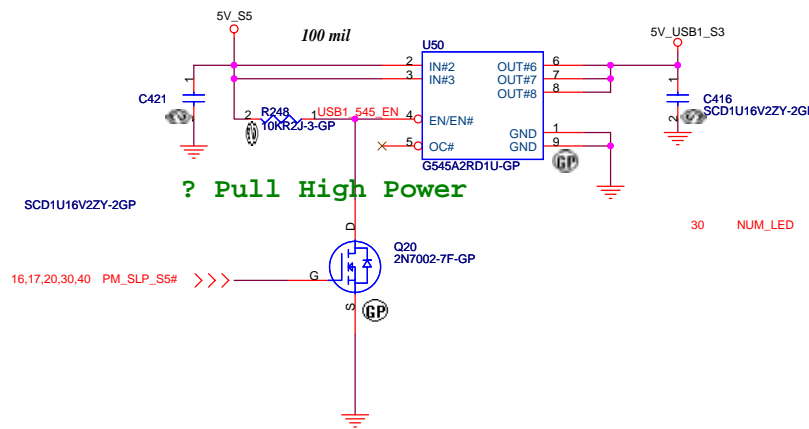
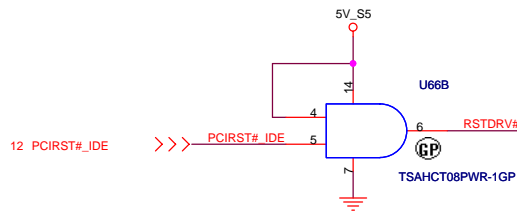
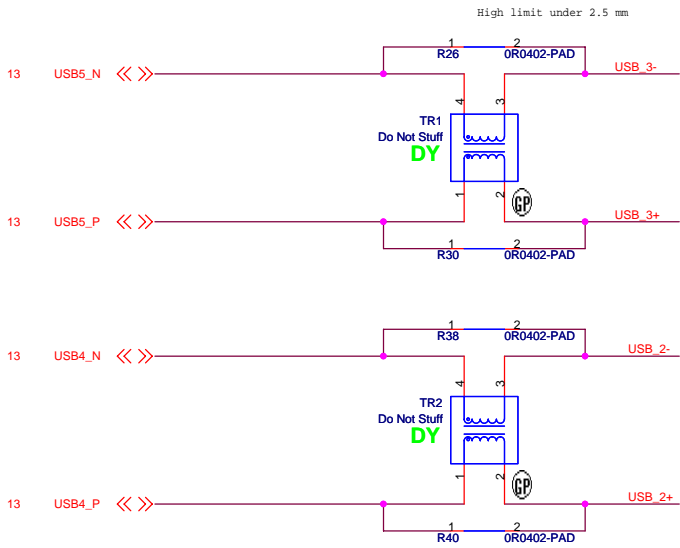
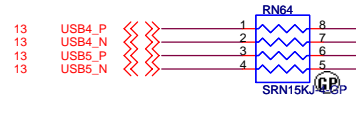
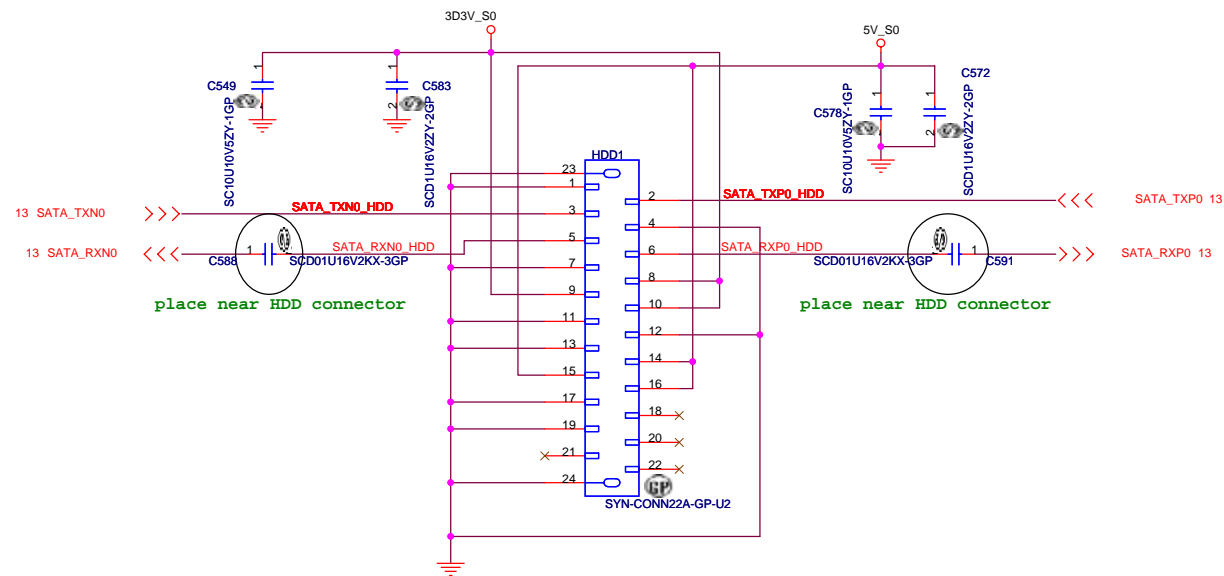




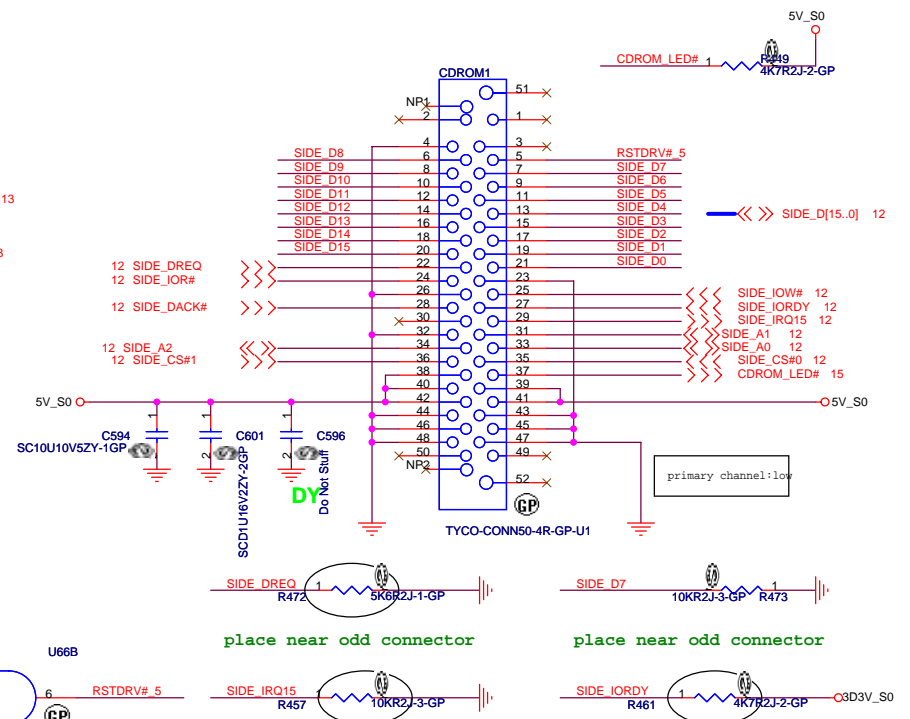
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<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Thermal/Fan Controller</b>	
Title Size Custom Date: Tuesday, August 14, 2007	Document Number <b>TIBET</b> Sheet 23 of 44
Rev <b>SA</b>	

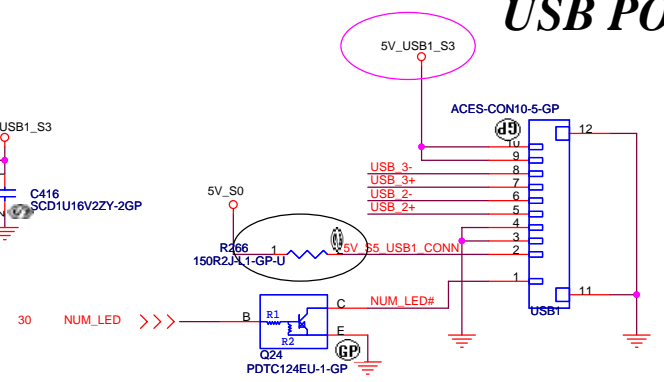
# SATA HD Connector



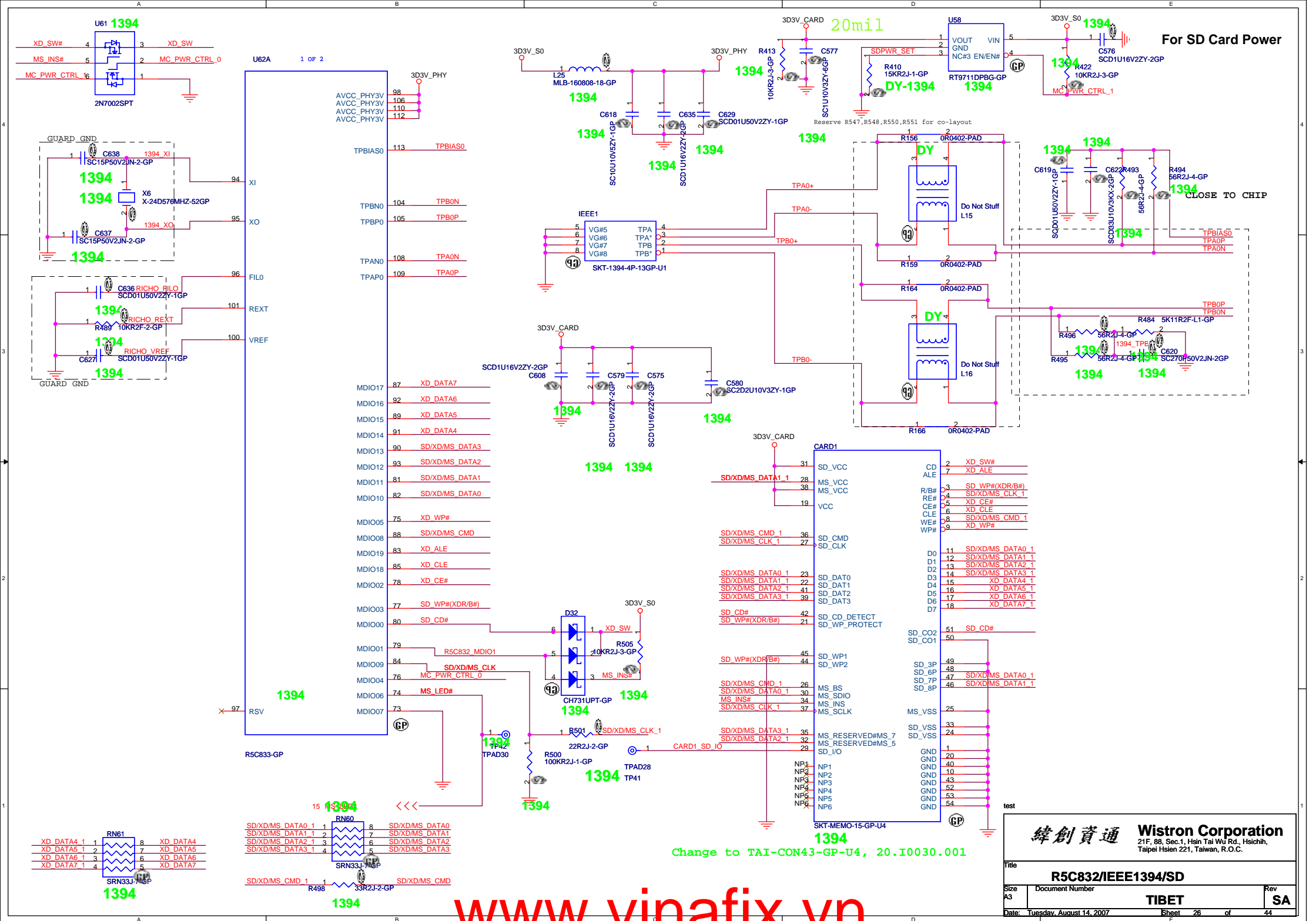
# CD-ROM CONNECTOR



# USB PORT

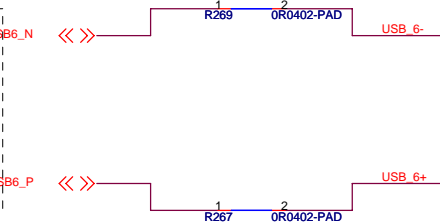
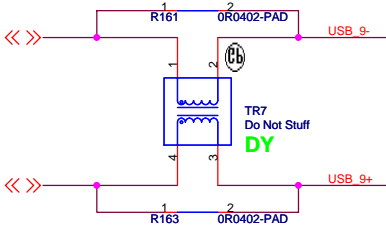
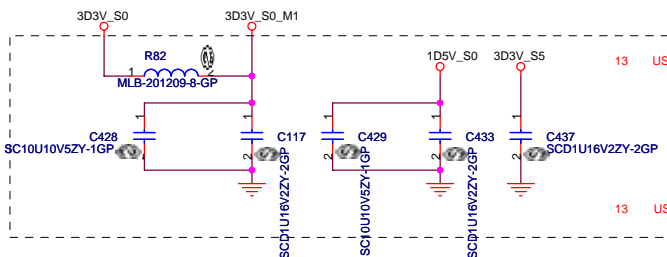
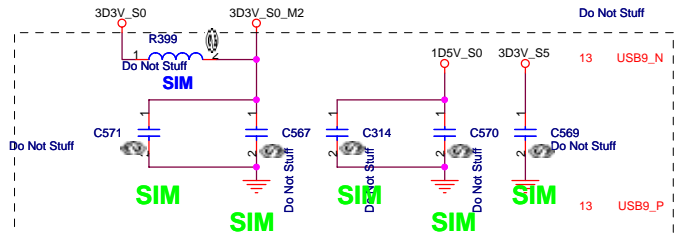
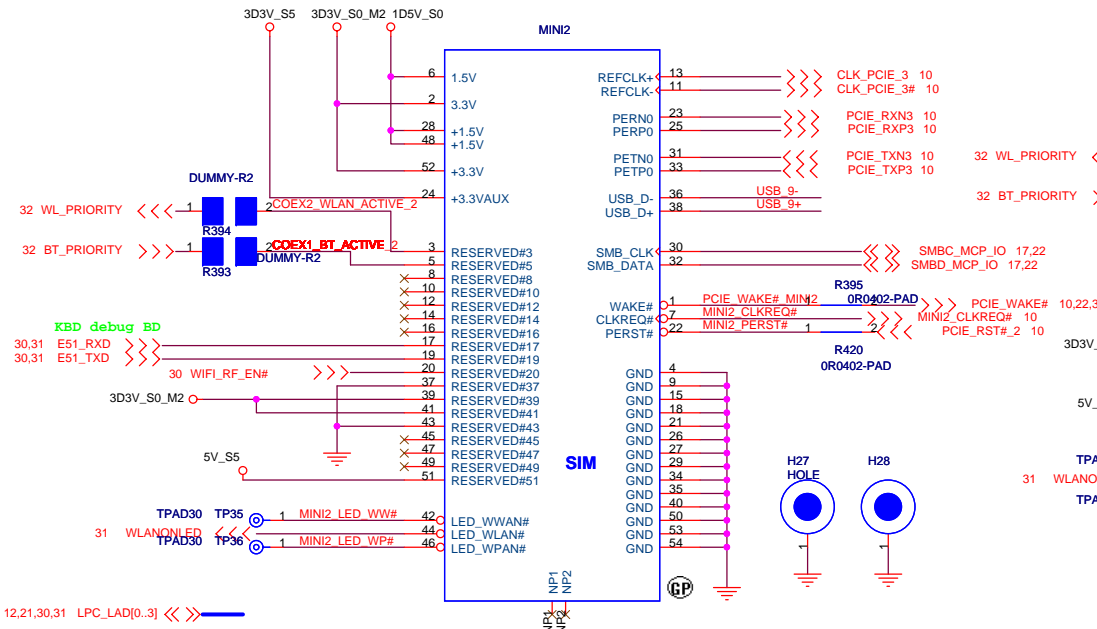


test



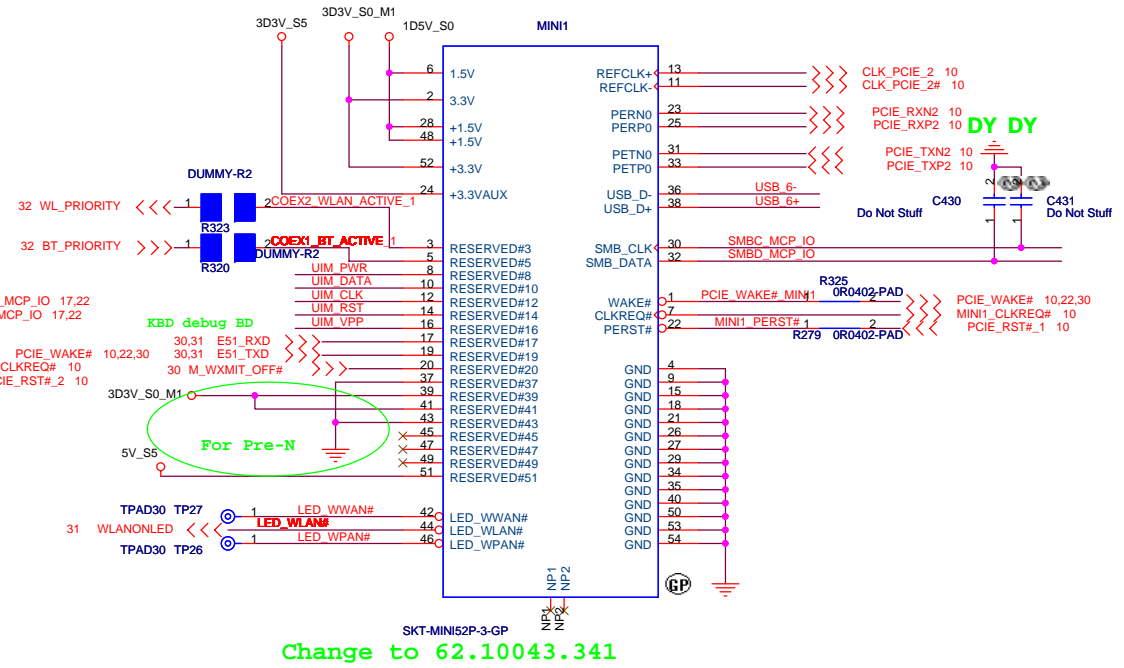
# Mini Card Connector 2

Wireless Card

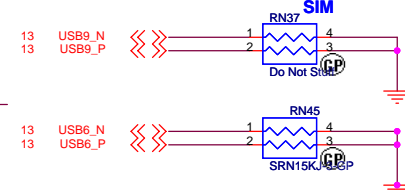
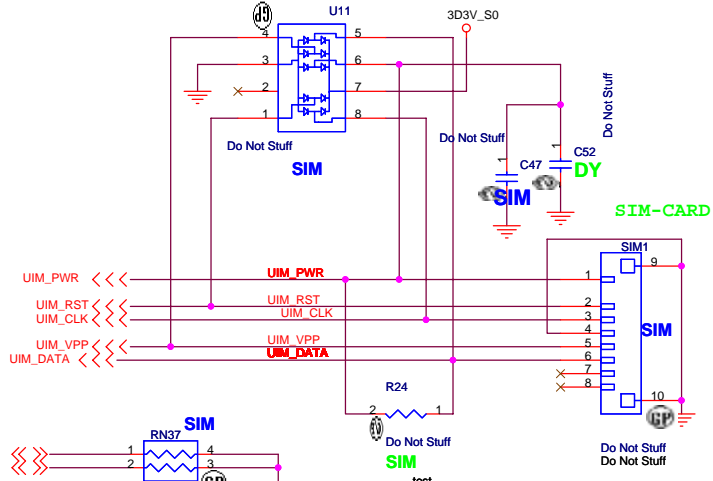


# Mini Card Connector 1

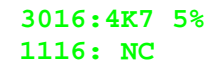
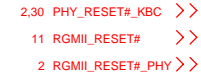
WWAN



Change to 62.10043.341



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[illegible]

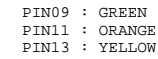
Change to 71.88318.003

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3016:2K 1%
1116: 4K99 1%
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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>LAN MARVELL 88E1116</b>			
Size A3	Document Number <b>TIBET</b>		Rev <b>SA</b>
Date: Tuesday, August 14, 2007		Sheet 28 of	44



**GIGA**



test

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
Title																													

LAN CONN

Size  
A3

Document Number
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## TIBET

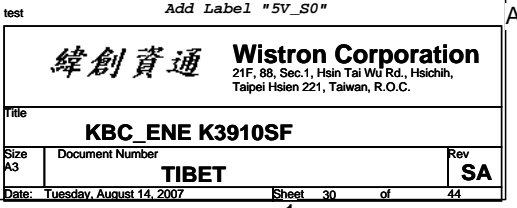
Rev  
SA

Date: Tuesday, August 14, 2007

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[www.vinafix.vn](http://www.vinafix.vn)



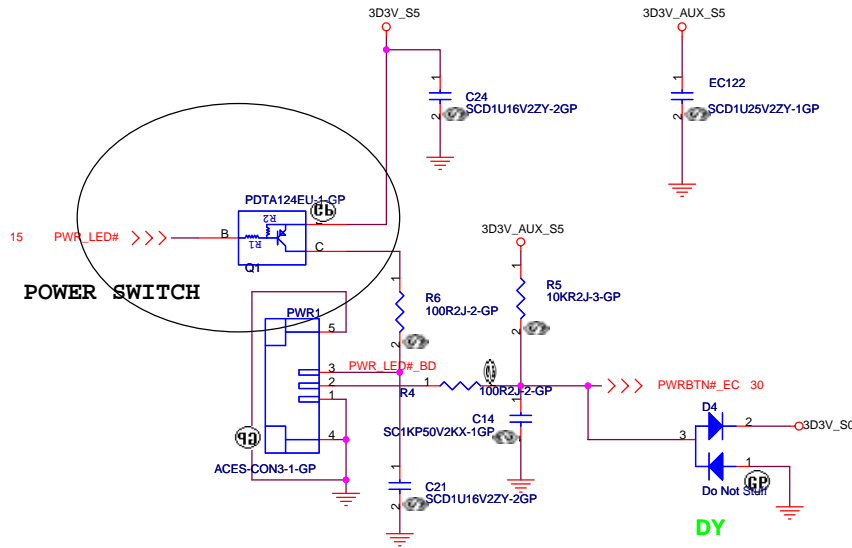


# GOLDEN FINGER FOR DEBUG BOARD

TOP VIEW

A15 (B1)  
A14 (B2)  
:  
:  
A2 (B14)  
A1 (B15)

(BOTTOM VIEW)

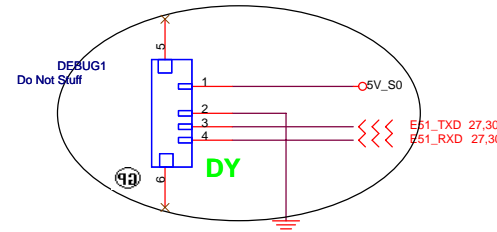
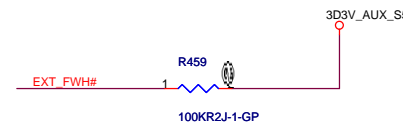
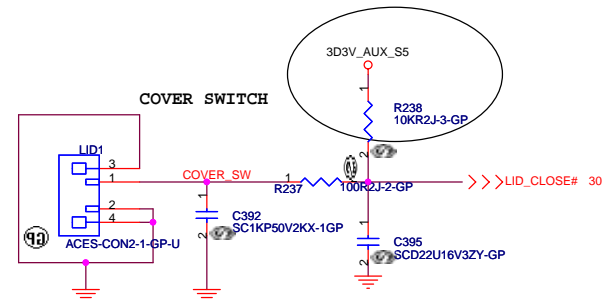


DY

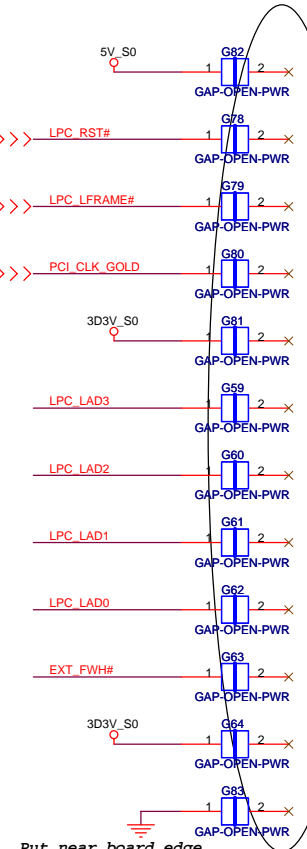
12,30 LPC\_RST# >>> LPC\_RST#

12,21,30 LPC\_LFRAME# >>> LPC\_LFRAME#

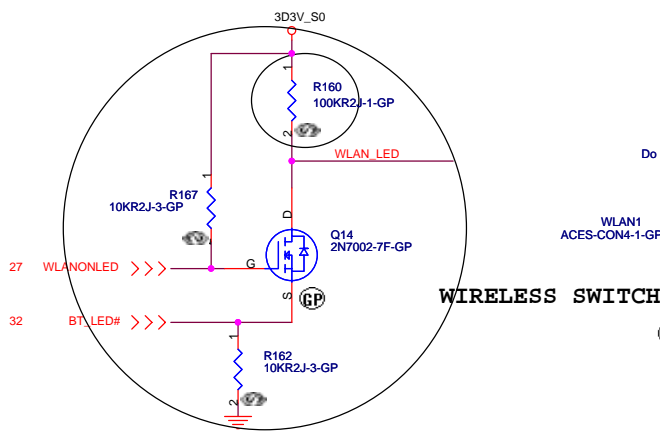
12 PCI\_CLK\_GOLD >>> PCI\_CLK\_GOLD



DY



Put near board edge  
test



DY

Do Not Stuff

WLAN1

ACES-CON4-1-GP

WLAN\_LED

WIRELESS\_BTN#\_R1

WIRELESS\_BTN# 30

WIRELESS\_BTN# 30

WIRELESS\_BTN# 30

WIRELESS\_BTN# 30

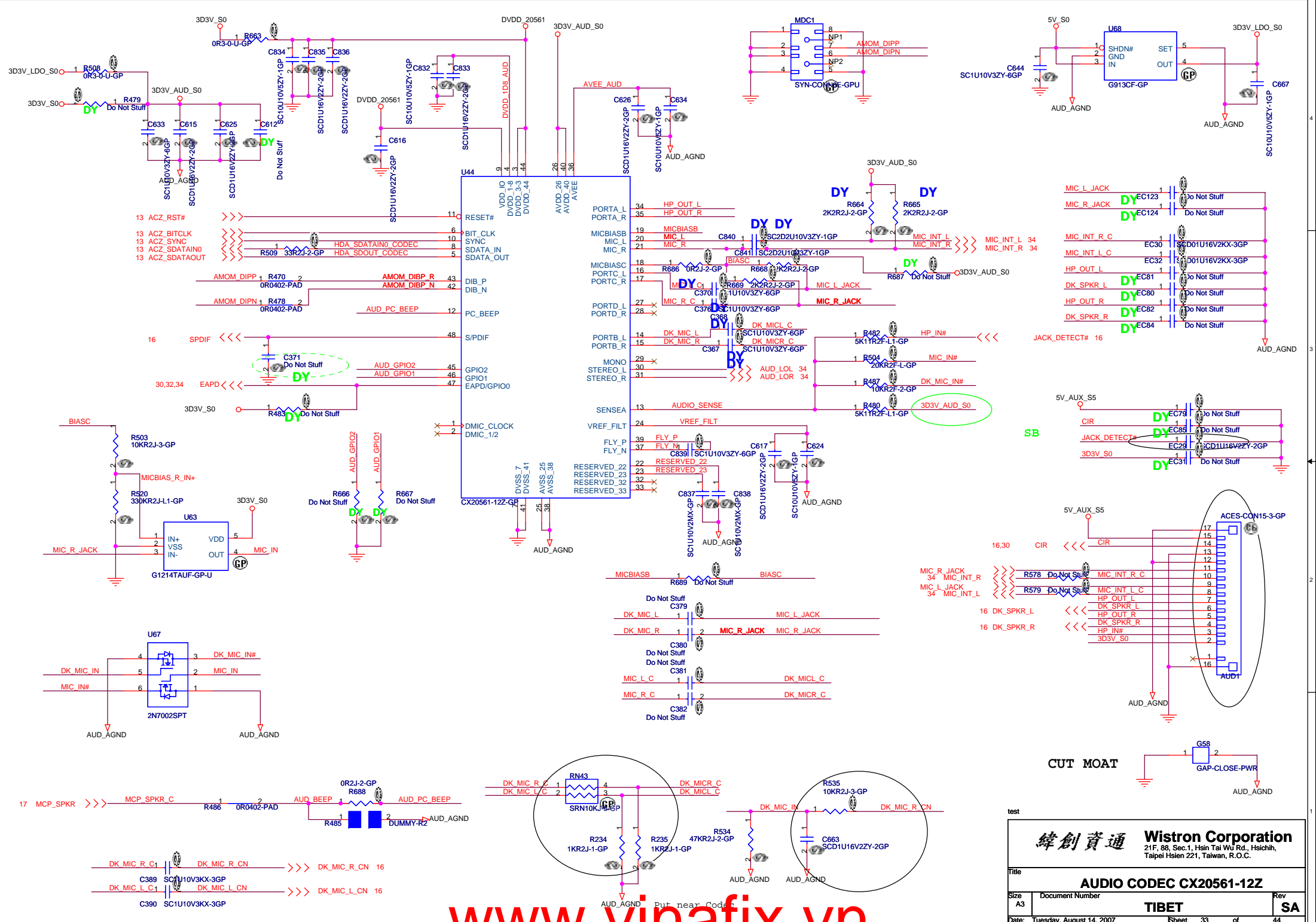
WIRELESS\_BTN# 30

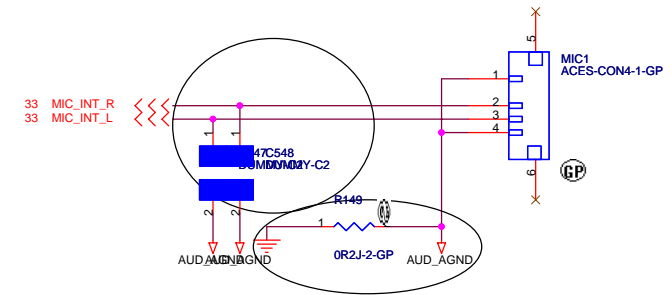
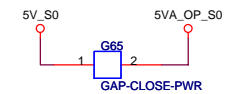
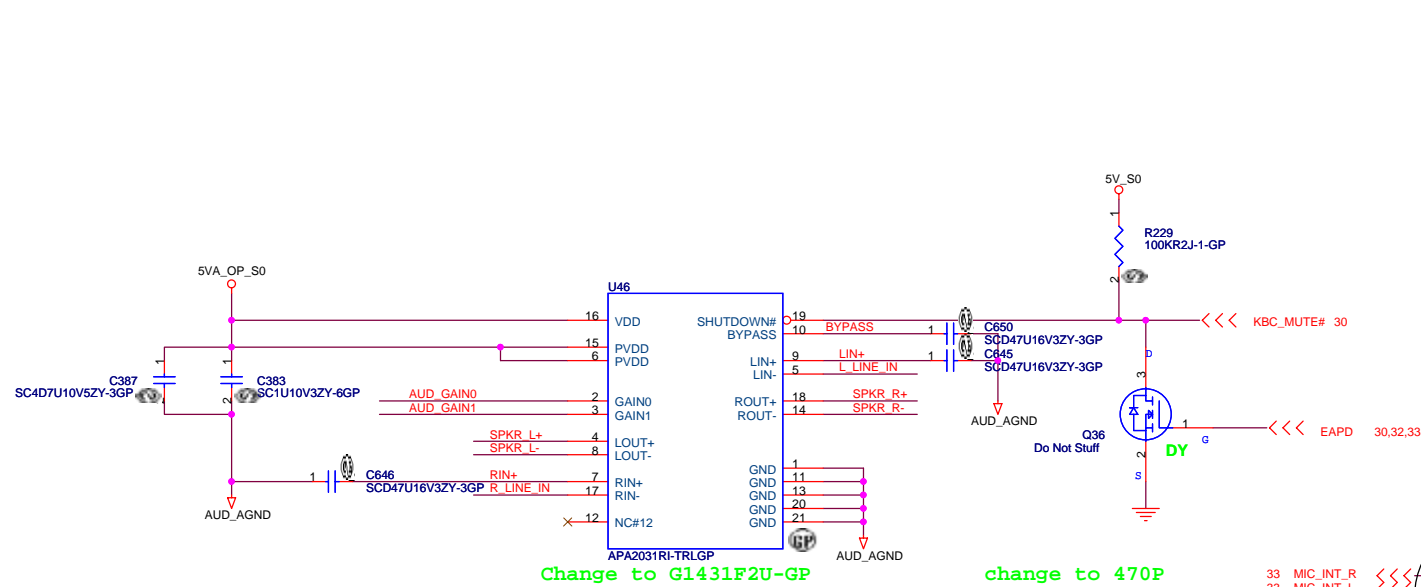
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

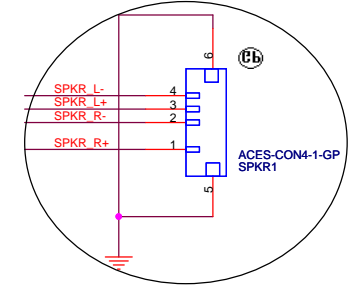
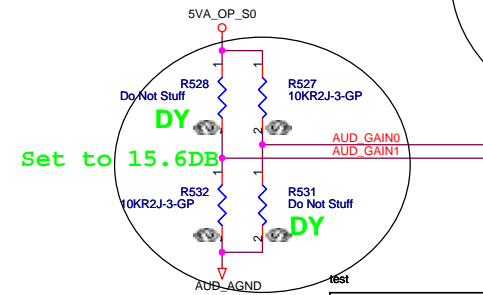
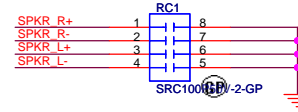
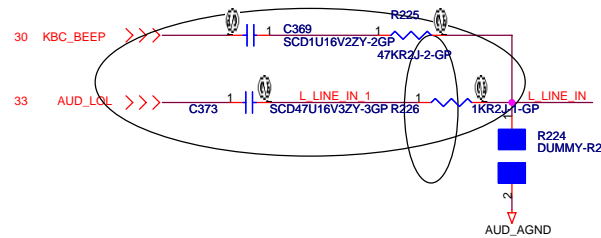
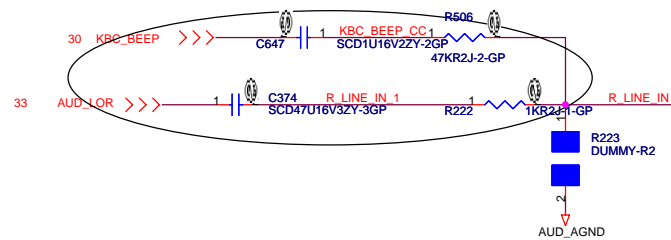
Title		
FLASH and Debug		
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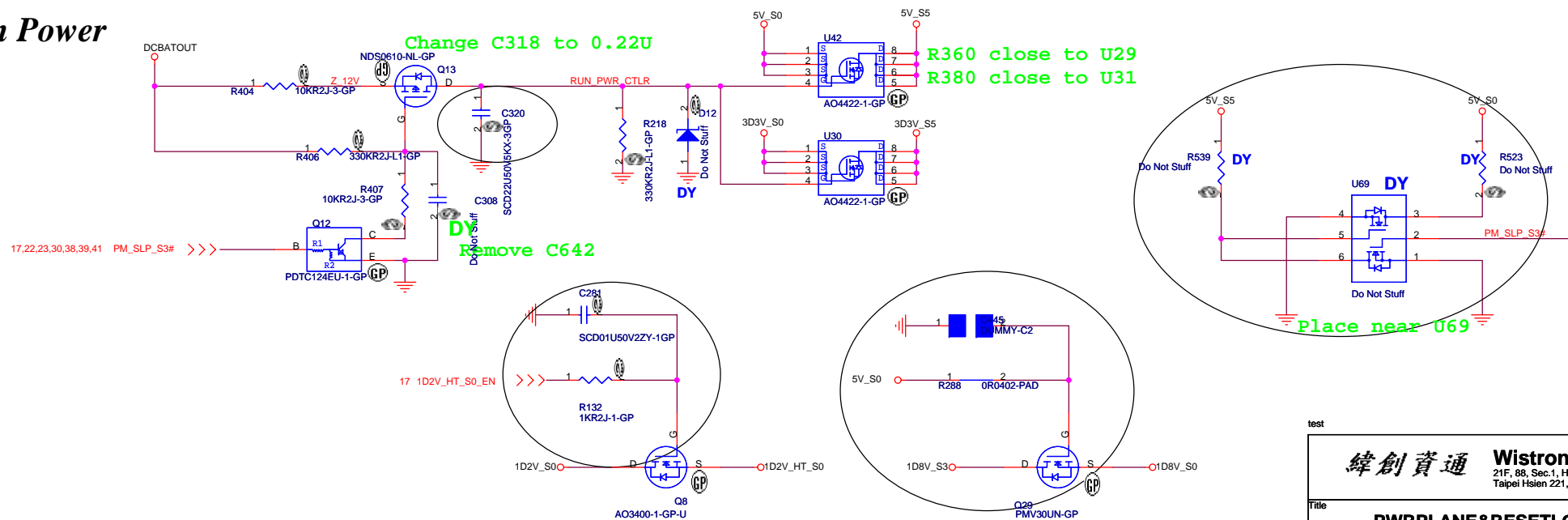
## Speaker



## Suspend Power

Remove Dummy PAD

## Run Power



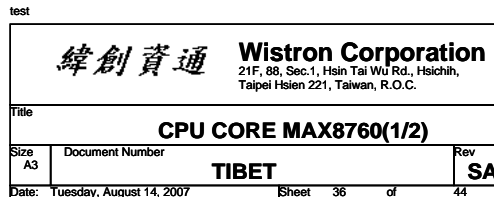
www.vinafix.vn

test

<b>緯創資通</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>PWRPLANE&amp;RESETLOGIC</b>			
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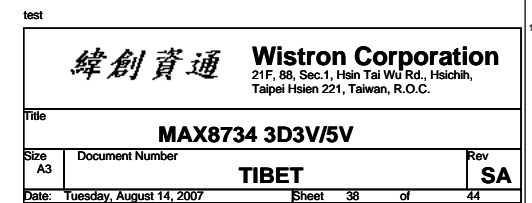
VID=1.15V(25W)/1.1V(35W)  
Iomax=25A(25W)/35A (35W)  
OCP=40A~45A

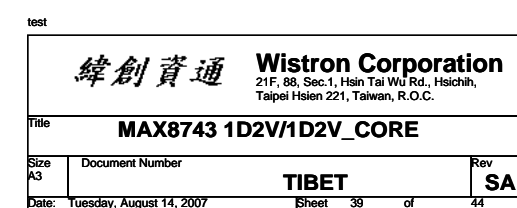
TON:	Frequency:
GND	550KHz
REF	300KHz
OPEN	200KHz
VCC	100KHz



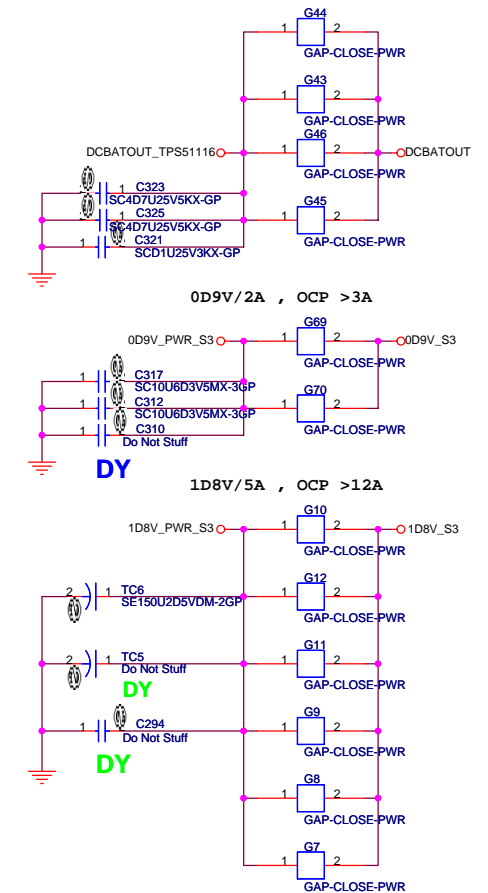
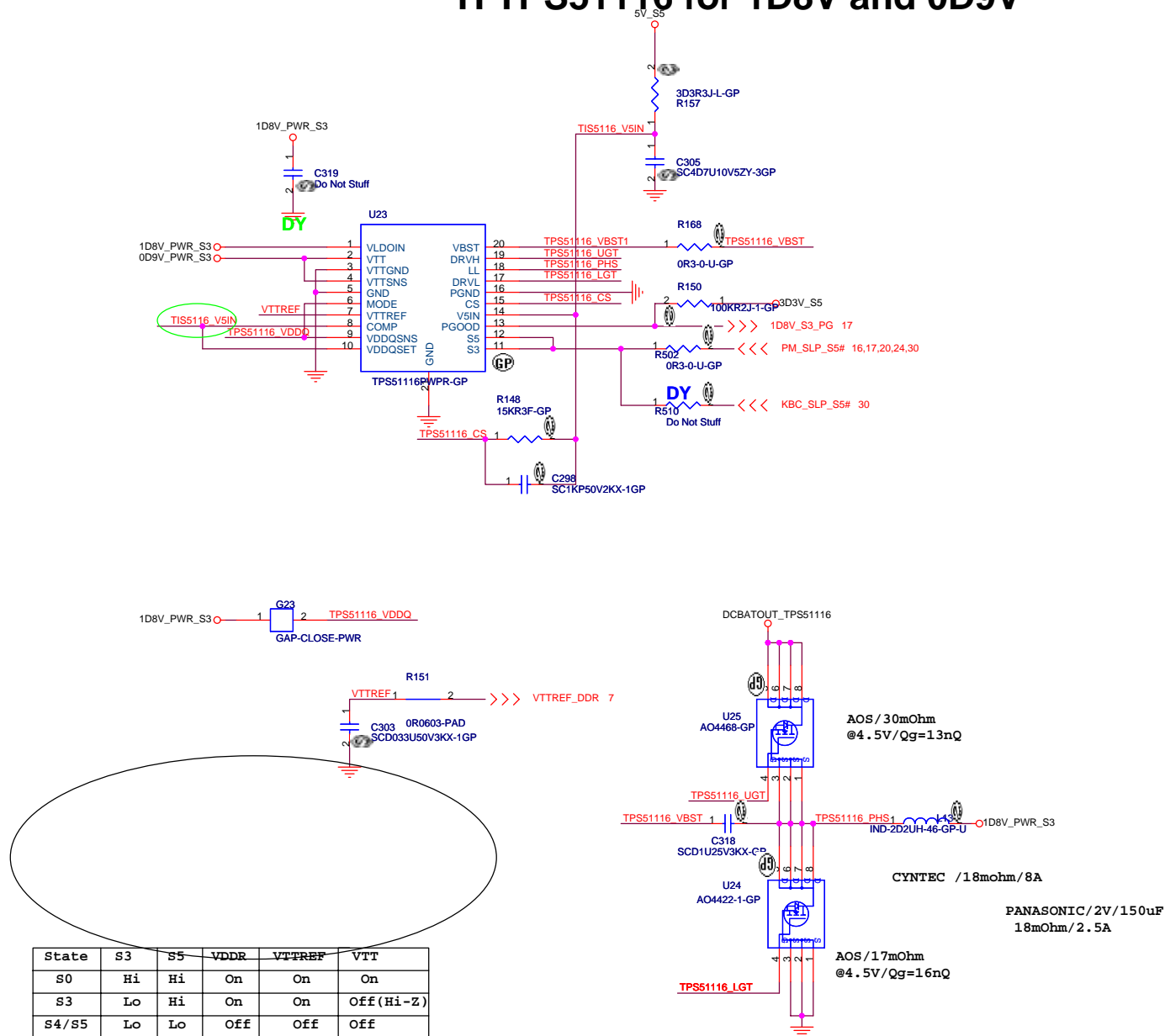




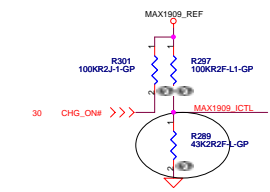




# TI TPS51116 for 1D8V and 0D9V

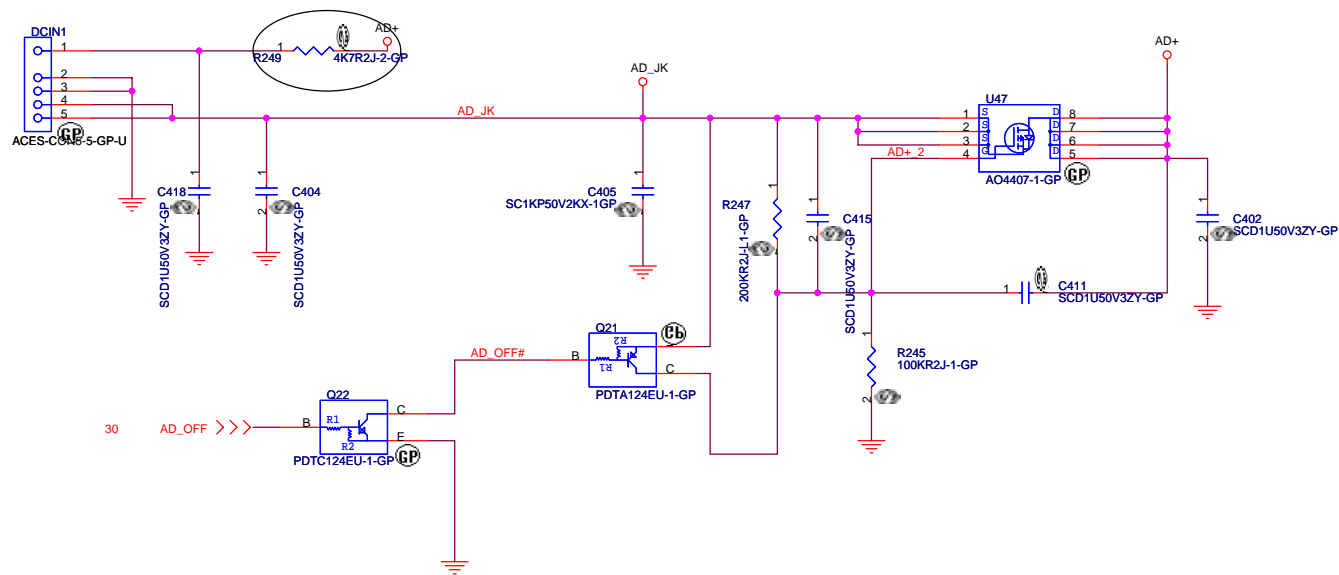




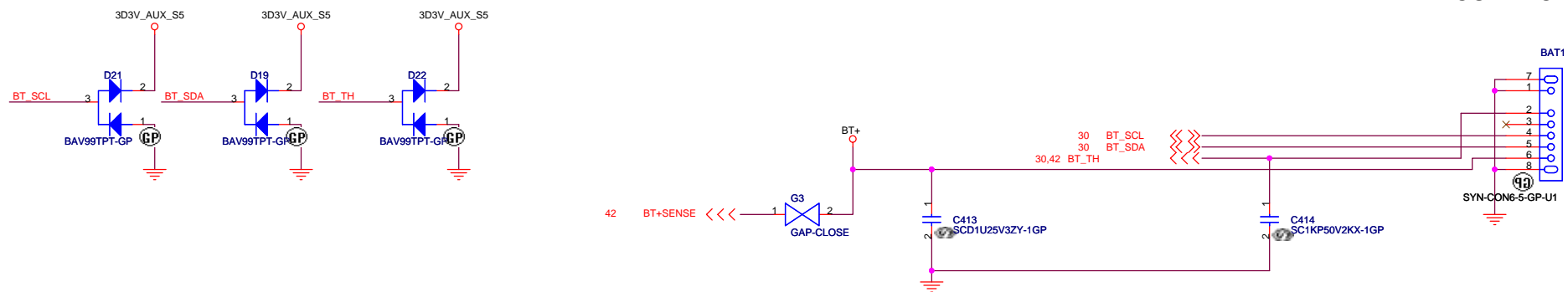


```
Pre-Charge :
MAX8725 : CHG_I_PRE_SEL = H,
Pre-Charge current = 300mA
```

## Adaptor in to generate DCBATOUT

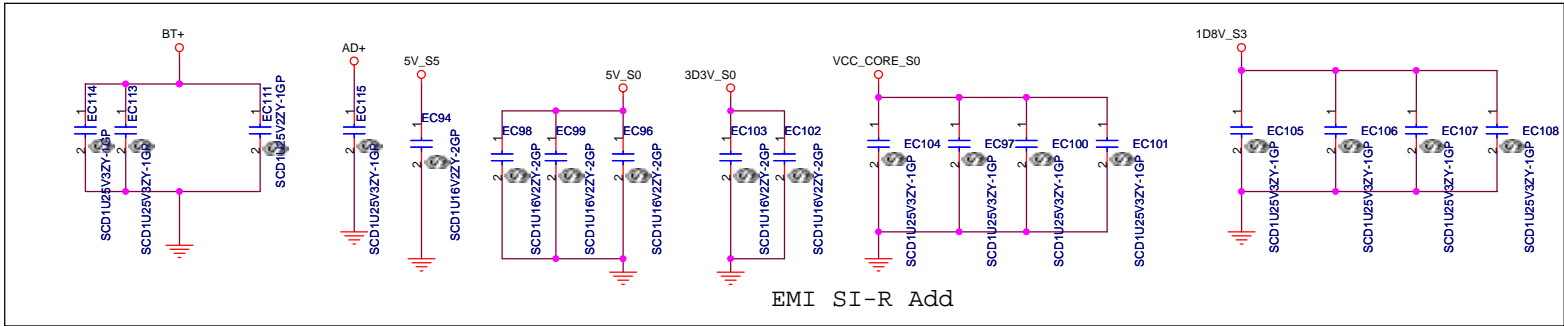


## BATTERY CONNECTOR

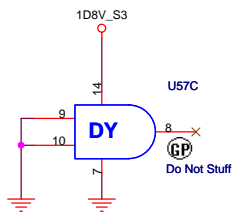
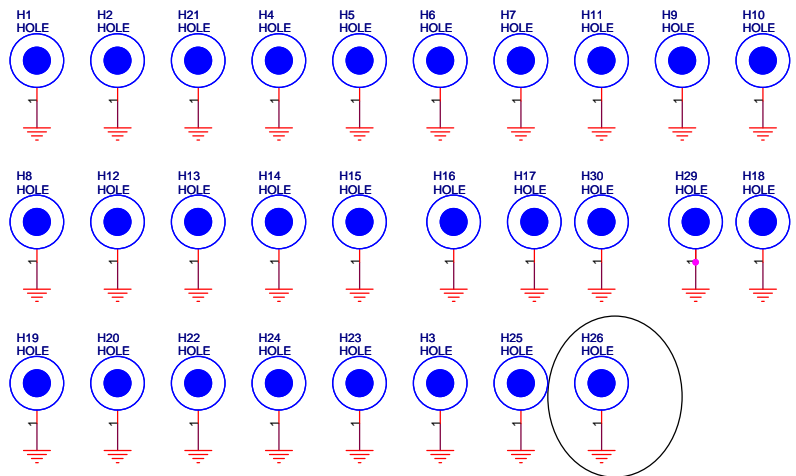
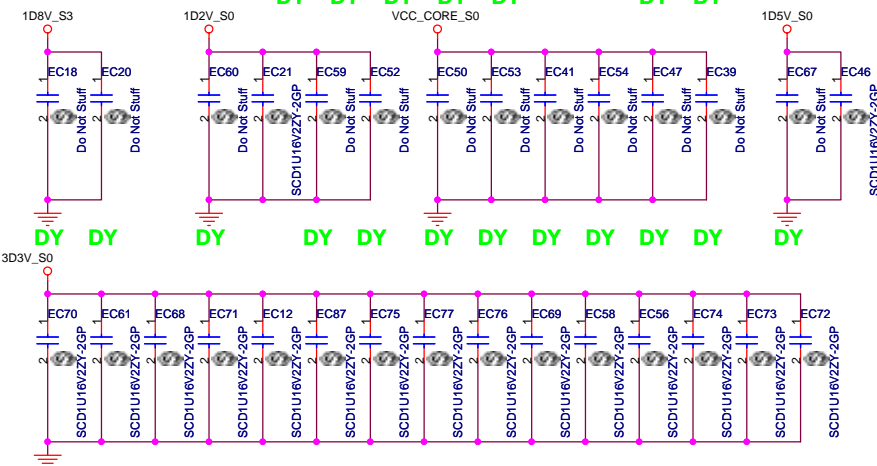
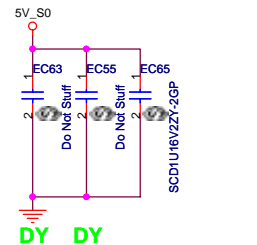
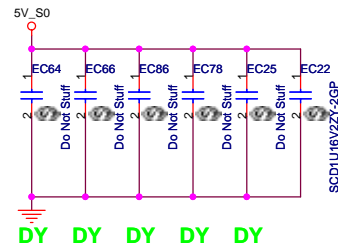
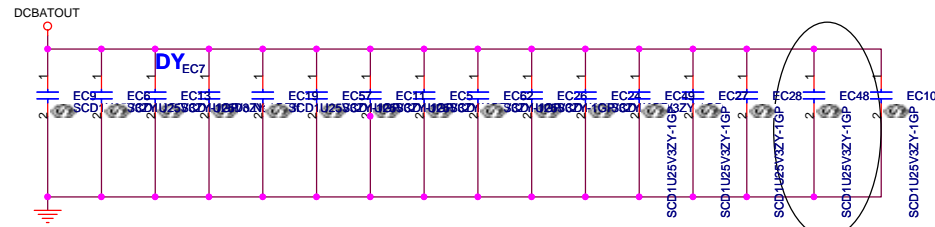
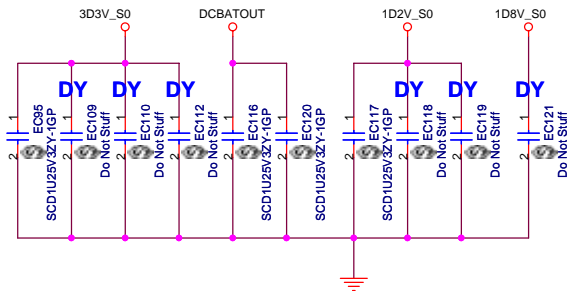


test

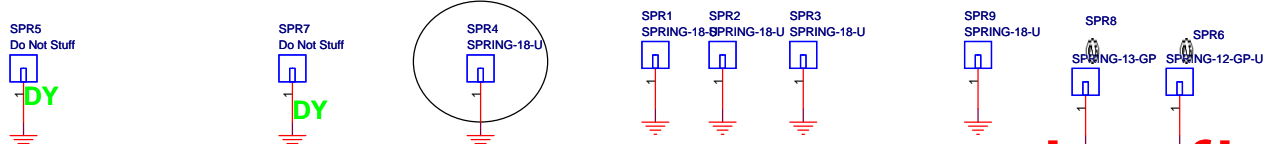
<b>緯創資通</b> <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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	FF	DF
CAMERA	○	×
LAN	10/100	10/100
1394/5 IN 1	○	×
EXTRA USB	○	×
MIC	○	×
CR LED	○	×



Modify SPR7 P/N manually



THE FOOTPRINT OF SPR5, SPR6, SPR7 CAN NOT BE GNT